SNLED2730 Series

USER'S MANUAL

SNLED2735F
SNLED27351J
SNLED27352J
SNLED2734X
SNLED27341J
SNLED27342J

SONiX Matrix LED Driver IC

AMENDENT HISTORY

Version	Date	Description
VER 1.0	2019/12/22	First version released.
VER 1.1	2020/02/18	1. Modify SDB pin Schmitt trigger structure as input mode only. 2. Modify Chapter3 Power state machine flow chart. 3. Modify Chapter4 I2C description ADDR/CS pin Connected to VDDIO. 4. Modify Chapter8 Application circuit, SDB connect Resistor to MCU. 5. Modify Chapter9 VDDIO ≤ VDD.
VER 1.2	2020/03/16	1. Modify Chapter11.1 LQFP 48PIN PKG information.
VER 1.3	2020/06/03	1. Add SNLED27342JG.
VER 1.4	2021/11/26	1. Modify Chapter3 Power State Machine Flow Chart 2. Modify Chapter6 Thermal register define. 3. Modify Chapter8 Application circuit diagram. 4. Modify operating ambient temperature.

Table of Content

1 PRODUCT OVERVIEW

1.1 FEATURES

- **LED Controls**
  Each LED has the on/off control.
  Each LED has the 8-bit programmable PWM duty.
  Each LED has the open/short detection status.
  De-ghost LED effects.

- **MPWM IO (CA1~CA16, CB1~CB12)**
  CA1~CA16 each IO supports maximum 40mA source constant current.
  CB1~CB12 each IO has 640mA sink current.
  Each MPWM IO supports staggered delay.
  Each MPWM IO supports slew rate control.

- **white balance current fine tune**
  Each CB channel has the current tune control.

- **Scan Phase Setting**
  Adjust scan phase in one frame

- **Matrix Control Engine**
  16-ch source and 12-ch sink MPWM I/O.
  Support 192 LEDs and 64 RGB LEDs.
  28.6KHz PWM frequency.

- **Support I2C/SPI slave communication**
  400KHz in I2C Slave mode.
  Support four auto-selective slave addresses by which ADDR pin are connected to (VDD/VSS/SCL/SDA).
  4MHz in SPI Slave write mode.
  CS pin control to enable SPI slave mode.

- **Support VDDIO for digital I/O power**

- **Thermal Detection**
  Support thermal shutdown at 150℃.
  Support thermal flag at 70℃.

- **Power Modes**
  Normal Mode
  Software shutdown mode.
  Software sleep mode.
  Hardware sleep mode.

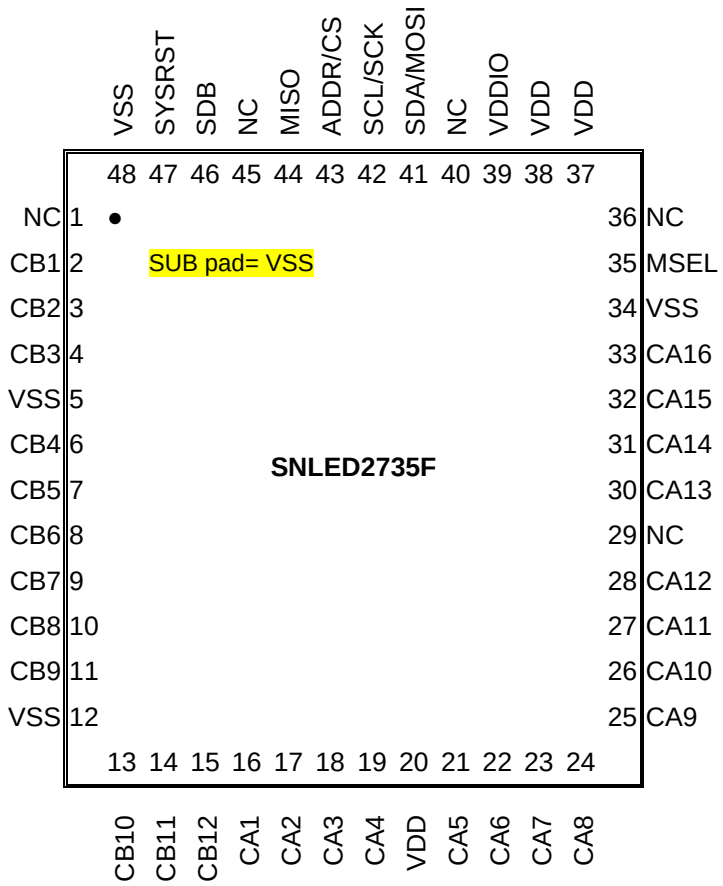
- **Package**
  LQFP48
  QFN40
  QFN32
  SSOP28

- **Features Selection Table**

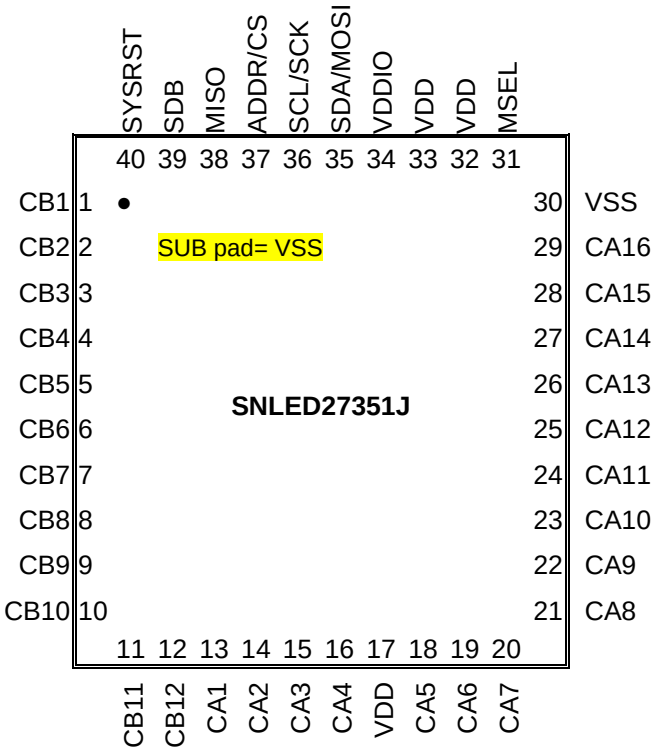
CHIP	I2C Slave	SPI Slave	MPWM IO (Source CH)	Sink CH	LED Matrix	Single LED	RGB LED	Operating Voltage	VDDIO	Package
SNLED2735	V	V	16-ch	12-ch	16*12	192	64	2.7V~5.5V	2.45V~5.5V	LQFP48
SNLED27351	V	V	16-ch	12-ch	16*12	192	64	2.7V~5.5V	2.45V~5.5V	QFN40
SNLED27352	V	V	12-ch	12-ch	12*12	144	48	2.7V~5.5V	2.45V~5.5V	QFN40
SNLED2734	V	V	15-ch	3-ch	15*3	45	15	2.7V~5.5V	2.45V~5.5V	SSOP28
SNLED27341	V	V	16-ch	6-ch	16*6	96	32	2.7V~5.5V	2.45V~5.5V	QFN32
SNLED27342	V	-	16-ch	12-ch	16*12	192	64	2.7V~5.5V	VDD	QFN32

1.2 PIN ASSIGNMENT

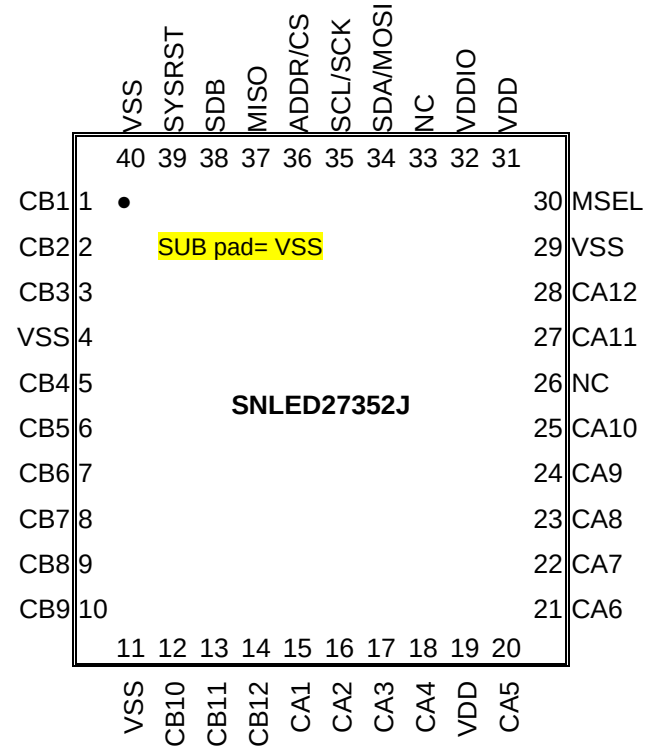
SNLED2735F (LQFP 48, 7x7x1.4MM): I2C & SPI Interface



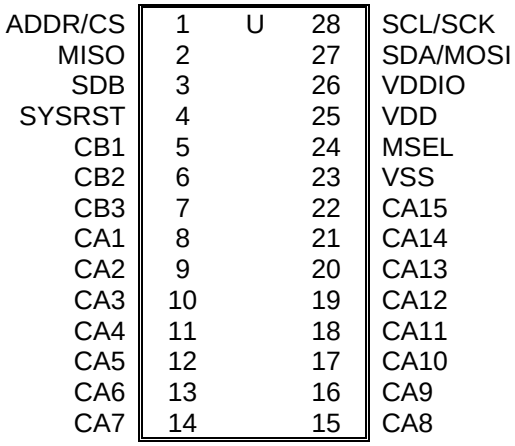
SNLED27351J (QFN40, 5x5x0.55MM): I2C & SPI Interface



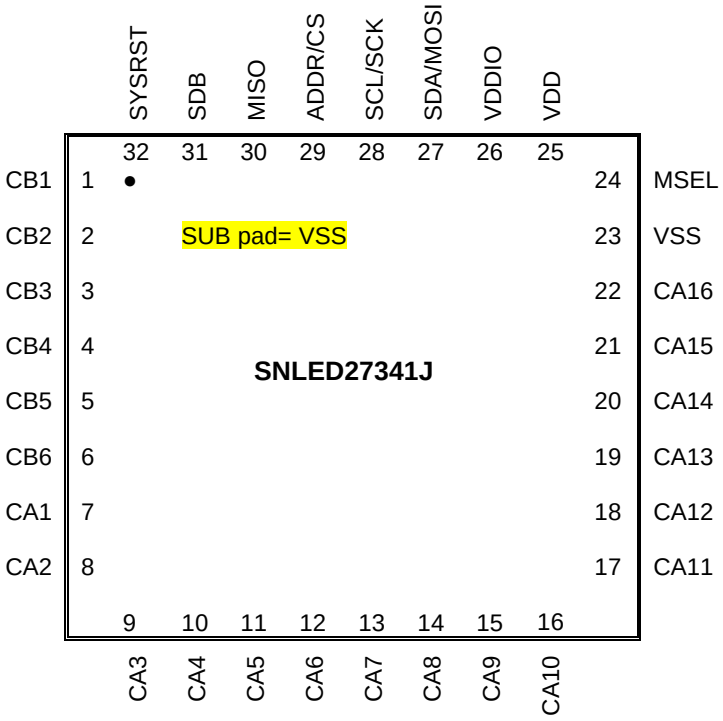
SNLED27352J (QFN40, 5x5x0.55MM): I2C & SPI Interface



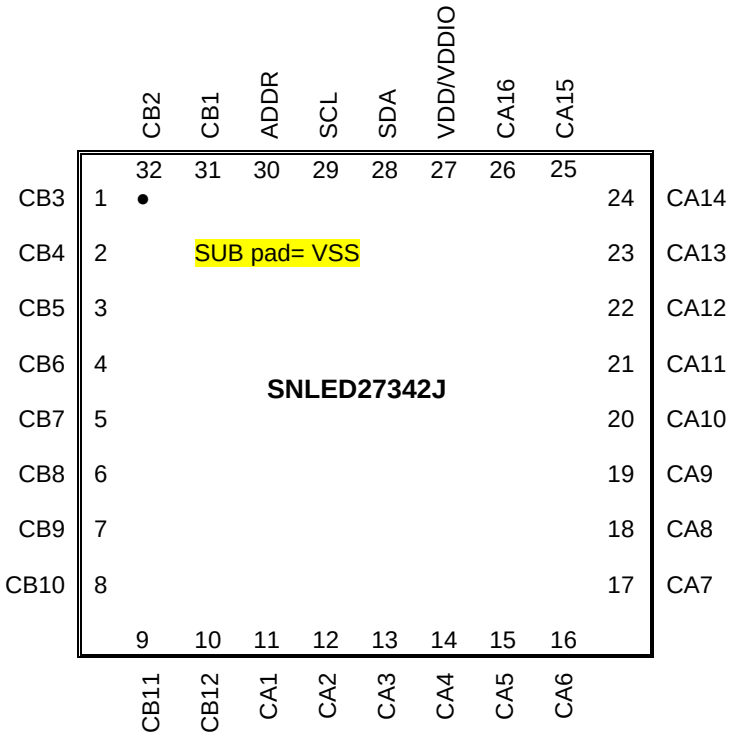
SNLED2734X (SSOP28, 209MIL): I2C & SPI Interface



SNLED27341J (QFN32, 4x4x0.55MM): I2C & SPI Interface



SNLED27342J (QFN32, 4x4x0.55MM): I2C Interface



1.3 PIN DESCRIPTIONS

PIN NAME	TYPE	DESCRIPTION
VDD	P	Power supply input pin for analog circuit.
VDDIO	P	Power supply input pad for the IO power of SDB, SYSRST, MISO, ADDR/CS, SDA/MOSI, SCL/SCK.
VSS	P	Ground pin for analog and digital circuit.
MSEL	I	Mode selection pin for I2C or SPI interface. Input only pin. I2C mode: MSEL tie GND. SPI mode: MSEL tie VDD.
SDB	I	Schmitt trigger structure as input mode only. Hardware power down the chip when pull to low.
SYSRST	I	System reset pin with internal pull-up resistor. System reset the chip when pull to low.
MISO	I	MISO: SPI Master-Input-Slave-Output pin. It's input floating pin and should tie to GND when I2C mode.
ADDR/CS	I	ADDR: I2C slave address selection pin. Schmitt trigger structure as input mode.
		CS: Slave chip select input pin in SPI mode. Low active. Schmitt trigger structure as input mode.
SDA/MOSI	I/O	SDA: I2C compatible serial data pin. Open drain IO. Schmitt trigger structure as input mode.
		MOSI: SPI Master-Output-Slave-Input pin. Schmitt trigger structure as input mode.
SCL/SCK	I/O	SCL: I2C compatible serial clock pin. Open drain IO. Schmitt trigger structure as input mode.
		SCK: SPI Clock input pin. Schmitt trigger structure as input mode.
CA1~CA16	O	PWM pin with constant current source.
CB1~CB12	O	Sink pin for LED matrix scan.

2 ARCHITECTURE DESCRIPTOR

2.1 RAM MAPPING

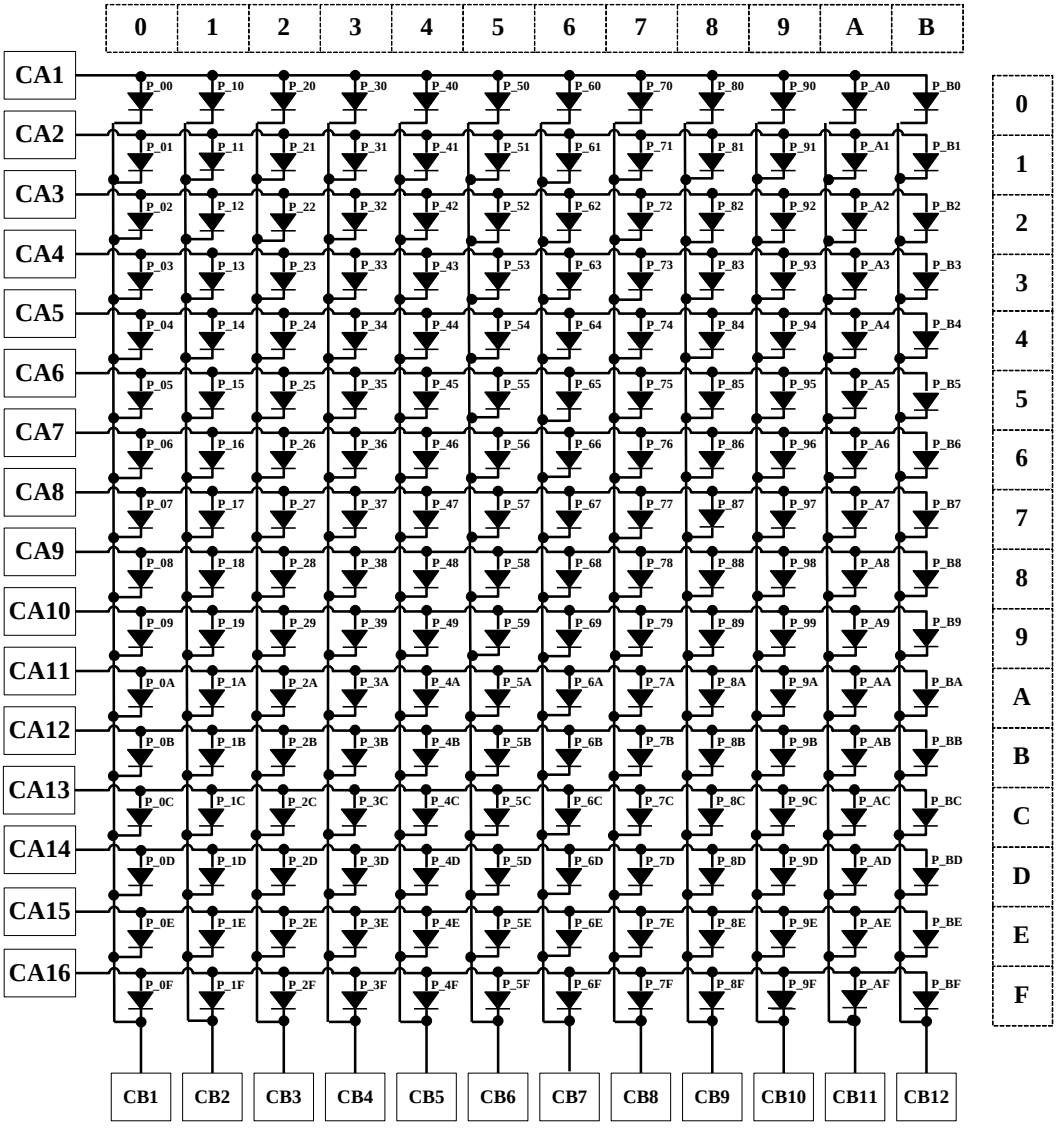
Page No.	User Address	*Register Segment*	Comment
↑	000H		
	...	***LED Control Register***	24-byte
	017H		
	018H		
Page 0	...	***LED Open Register***	24-byte
	02FH		
	030H		
	...	***LED Short Register***	24-byte
↓	047H		
↑	000H		
Page 1	...	***PWM Register***	192-byte
↓	0BFH		
↑	000H		
Page 3	...	***Function Register***	27-byte
↓	01AH		
↑	000H		
Page 4	...	***LED Current tune Register***	12-byte
↓	00BH		

Note:

In I2C mode, user has to first configure the Command Register (FDh) with the following data 0x00, 0x01, 0x03 or 0x04 to select the Page Number.

2.2 RAM MAP

LED-Matrix (16*12)					
	Page 0			Page 1	Page 4
LED Location	LED Control Register	LED Open Register	LED Short Register	PWM Register	LED Current tune Register
CB1(P_00~P_0F)	00h + 01h	18h + 19h	30h + 31h	00h ~ 0Fh	00h
CB2(P_10~P_1F)	02h + 03h	1Ah + 1Bh	32h + 33h	10h ~ 1Fh	01h
CB3(P_20~P_2F)	04h + 05h	1Ch + 1Dh	34h + 35h	20h ~ 2Fh	02h
CB4(P_30~P_3F)	06h + 07h	1Eh + 1Fh	36h + 37h	30h ~ 3Fh	03h
CB5(P_40~P_4F)	08h + 09h	20h + 21h	38h + 39h	40h ~ 4Fh	04h
CB6(P_50~P_5F)	0Ah + 0Bh	22h + 23h	3Ah + 3Bh	50h ~ 5Fh	05h
CB7(P_60~P_6F)	0Ch + 0Dh	24h + 25h	3Ch + 3Dh	60h ~ 6Fh	06h
CB8(P_70~P_7F)	0Eh + 0Fh	26h + 27h	3Eh + 3Fh	70h ~ 7Fh	07h
CB9(P_80~P_8F)	10h + 11h	28h + 29h	40h + 41h	80h ~ 8Fh	08h
CB10(P_90~P_9F)	12h + 13h	2Ah + 2Bh	42h + 43h	90h ~ 9Fh	09h
CB11(P_A0~P_AF)	14h + 15h	2Ch + 2Dh	44h + 45h	A0h ~ AFh	0Ah
CB12(P_B0~P_BF)	16h + 17h	2Eh + 2Fh	46h + 47h	B0h ~ BFh	0Bh

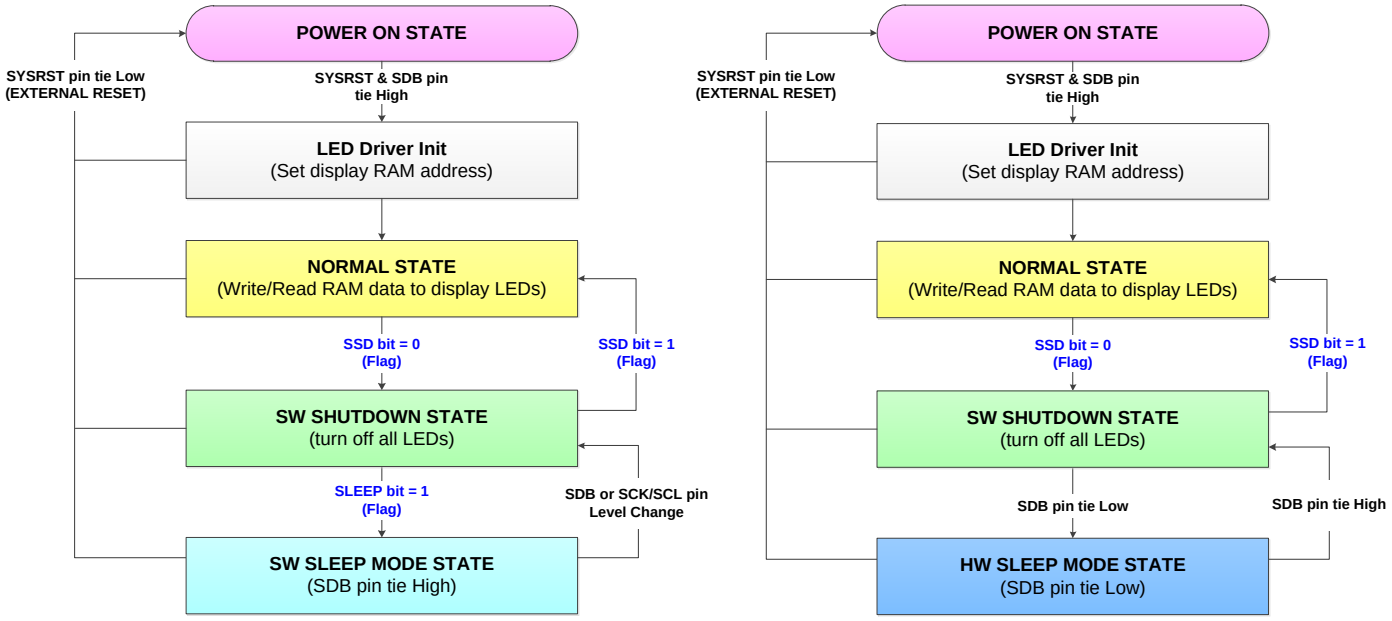


Matrix: 16*12

3 SYSTEM OPERATION MODE

3.1 POWER STATE MACHINE FLOW CHART

Power states are determined by the power on state, the software shutdown state (SSD bit), the hardware sleep state (SDB pin), and the software sleep register (SLEEP bit).



3.1.1 POWER ON STATE

When the VDD power is over V_{LVD} threshold, a power on initial sequence is executed. During the sequence, all registers are initialized to the default value.
After the sequence, the system will enter the SW POWER DOWN state if SDB pin is HIGH or will enter the HW POWER DOWN state if the SDB pin is LOW.

3.1.2 SW SHUTDOWN STATE

In this state, all current sources and digital drivers are switched off, so that the matrix is blanked. All registers and the SRAM data can be written or read. Normal mode requires 16us into software power down mode, and 128us wakeup time from software power down mode.

3.1.3 HW SLEEP MODE STATE

In this state, besides all current sources and digital drivers are switched off, all registers are forbidden writing and reading. Normal mode requires 16us into hardware power down mode, and 128us wakeup time from hardware power down mode.

3.1.4 SW SLEEP MODE STATE

In this state, besides all current sources and digital drivers are switched off, all registers are forbidden writing and reading. Normal mode requires 16us into sleep mode.

SCL(SCK), SYSRST and SDB are served as wakeup pins. The wakeup pins level change will be wakeup from sleep mode. The system wakeup time is 128us.

3.1.5 NORMAL STATE

In this state, all current sources and digital drivers are operating depending on the register settings.

3.1.6 EXTERNAL RESET

The external reset I/O is SYSRST pin. The SYSRST pin has internal Pull-up resistor. External reset will be trigger need keep low pulse more than 256us for SYSRST pin. The system reset time is 20ms.

The external reset after initialization as follows.

- All registers are set to their default value.
- The LED display will be turn off(software shutdown mode).

4 I2C SLAVE INTERFACE

For SNLED2735, when MSEL pin status is low, the system is in I2C Slave mode, and disables the SPI slave function. SNLED2735 uses a serial bus, which conforms to the I2C protocol, to control the chip's function with two wires: SCL and SDA. The 7-bit slave address Bit[7:1], followed by the R/W Bit[0]. Set Bit[0] to "0" for a write command and set Bit[0] to "1" for a read command. The value of Bit[2:1] is decided by the connection of the ADDR/CS pin.

Slave Address (Write only):

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Value	**1**	**1**	**1**	**0**	**1**	**AD_CON**		**0/1**
ADDR/CS pin Connected to GND, AD_CON = 00								
ADDR/CS pin Connected to VDDIO, AD_CON = 11								
ADDR/CS pin Connected to SCL, AD_CON = 01								
ADDR/CS pin Connected to SDA, AD_CON = 10								

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typical 1Kohm). The maximum clock frequency is 400KHz. In this discussion, the master is the microcontroller and the slave is SNLED2735.

The timing diagram for the I2C is shown in the figure below. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

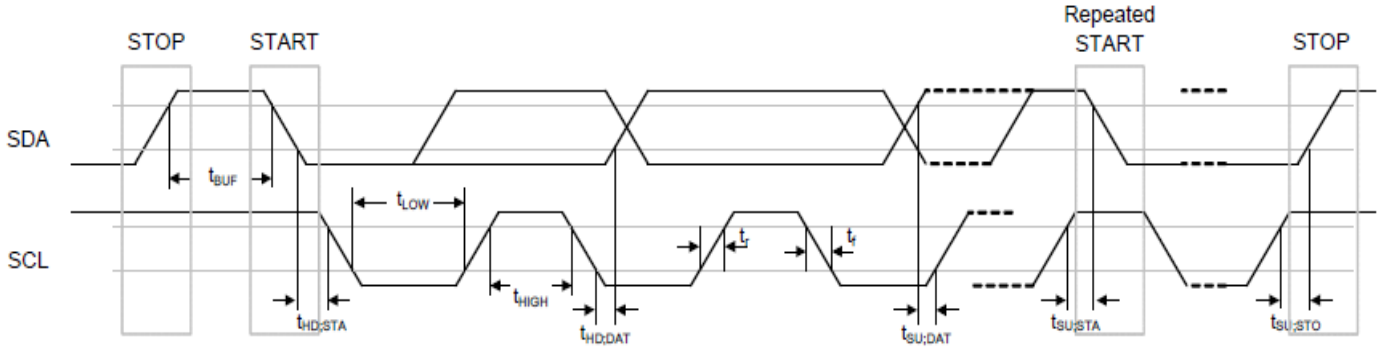
The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all device attached to the I2C bus to check the incoming address against their own slave address.

The 8-bit slave address is sent next, MSB first. Each address bit must be stable while the SCL level is high.

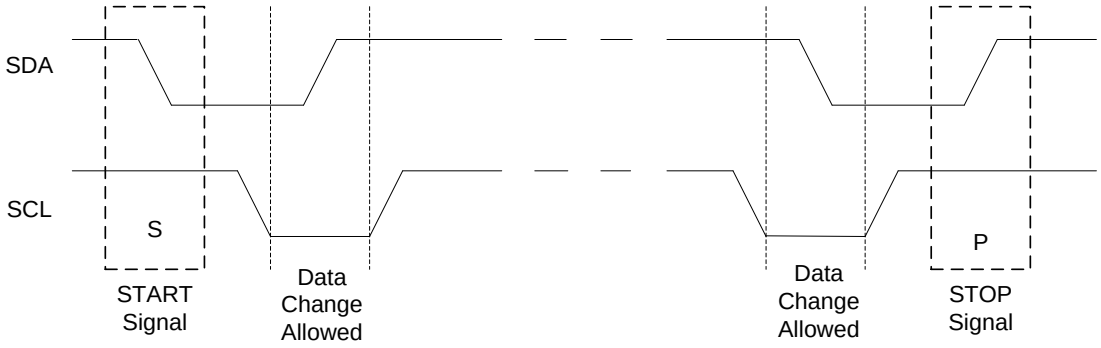
After the last bit of the chip address is sent, the master checks for the slave's acknowledge. The master releases the SDA line high (through a pull-up resistor.) Then the master sends an SCL pulse. If the slave has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal and abort the transfer. Following acknowledge of the slave, the register address byte is sent, MSB first. SNLED2735 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, MSB first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the slave must generate another acknowledge to indicate that the data was received.

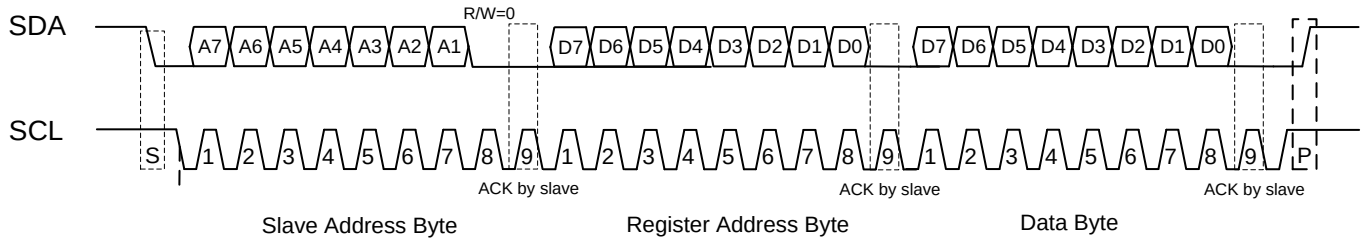
The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.



Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCL}	Serial-Clock frequency	-	-	400	kHz
t_{BUF}	Bus free time between a STOP and a START condition	1.3	-	-	us
$t_{HD,STA}$	Hold Time (repeated) START condition	0.6	-	-	us
$t_{SU,STA}$	Repeated START condition setup time	0.6	-	-	us
$t_{SU,STO}$	STOP condition setup time	0.6	-	-	us
$t_{HD, DAT}$	Data hold time	-	-	0.9	us
$t_{SU,DAT}$	Data setup time	100	-	-	ns
t_{LOW}	SCL clock low period	1.3	-	-	us
t_{HIGH}	SCL clock high period	0.7	-	-	us
t_R	Rise time of both SDA and SCL signals, receiving		20	300	ns
t_F	Fall time of both SDA and SCL signals, receiving		20	300	ns



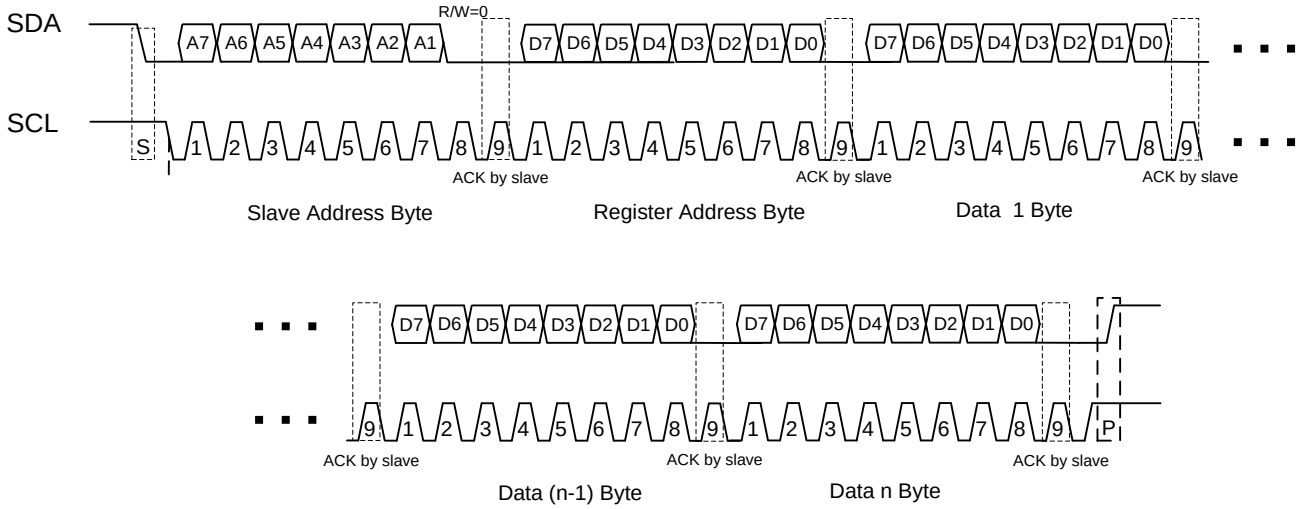
Bit transfer



Write to SNLED2735

4.1 ADDRESS AUTO INCREMENT

To write multiple bytes of data into SNLED2735, load the address of the data register that the first data byte is intended for. During SNLED2735 acknowledge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to SNLED2735 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to SNLED2735.



Write to SNLED2735 (Automatic address increment)

4.2 READING REGISTERS

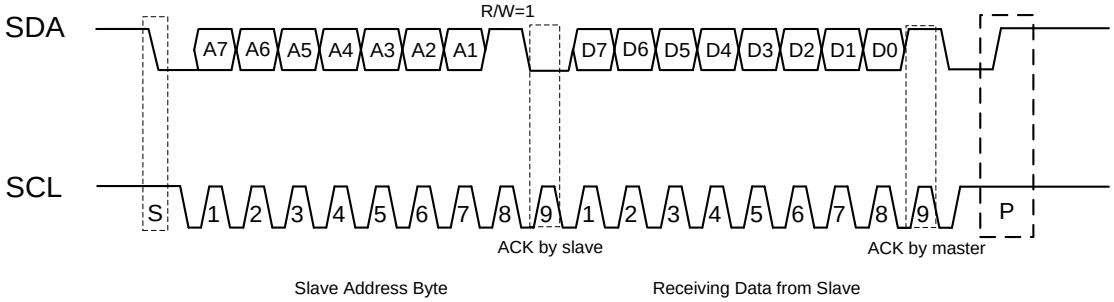
All of registers in SNLED2735 can be read. But frame Registers can only be read in software shutdown mode as SDB pin high. The Function Register and the Detection Register can be read in software shutdown mode or normal operating mode.

To read the device data, the bus master must follow the steps below:

1. Select the response register: Send the slave address with R/W bit set to “0”, followed by the Command Register address, FDH, then send command data which determines which response register is accessed. (This step can be ignored if the current response register is the same as the new one to be set.)

2. Set the address of the data to be read: Send the slave address with R/W bit set to “0”, followed by the address byte of the data to be read.

3. Read the data: Send the slave address with R/W bit set to “1” and then read the data.



Read from SNLED2735

5 SPI SLAVE INTERFACE

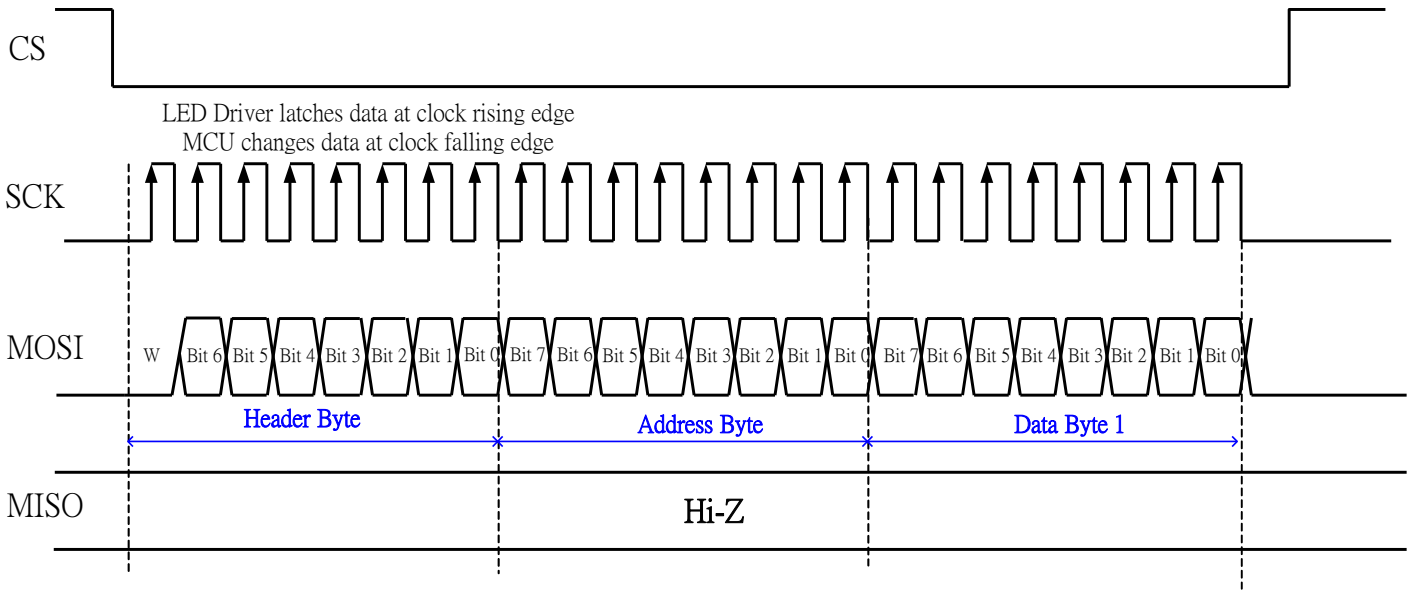
For SNLED2735, when MSEL pin status is high, the system is in SPI Slave mode, and disables the I2C slave function. SNLED2735 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI, and MISO. SPI transfer starts from CS pin from high to low controlled by Master (microcontroller), and SNLED2735 latches the data when clock rising

The SPI data format is 8-bit length. The first header byte composite of 1-bit R/W bit, 3-bit checking pattern and 4-bit Response Register must be sent first, and is followed by the following address byte that the data is to be accessed is sent. And if the R/W bit is "0", meaning a write operation, Master (micro-controller) can write the data byte to the address.

The maximum SCK frequency supported in SPI write mode is 4MHz.

Header byte (Write only):

Name	R/W Bit	Checking Pattern	Response Register
Bit	Bit 7	Bit 6:4	Bit 3:0
Value	**0: Write operation 1: Read operation**	**010 (Fixed)**	**0x0, Point to Page 0 (LED Control Register is available) 0x1, Point to Page 1 (PWM Register is available) 0x3, Point to Page 3 (Function Register is available) 0x4, Point to Page 4 (Current Tune Register is available)**



Write to SNLED2735

5.1 ADDRESS AUTO INCREMENT

To write multiple bytes of data into SNLED2735, load the address of the data register that the first data byte is intended for. After SNLED2735 receiving the data byte, the internal address pointer will increment by one. The next data byte

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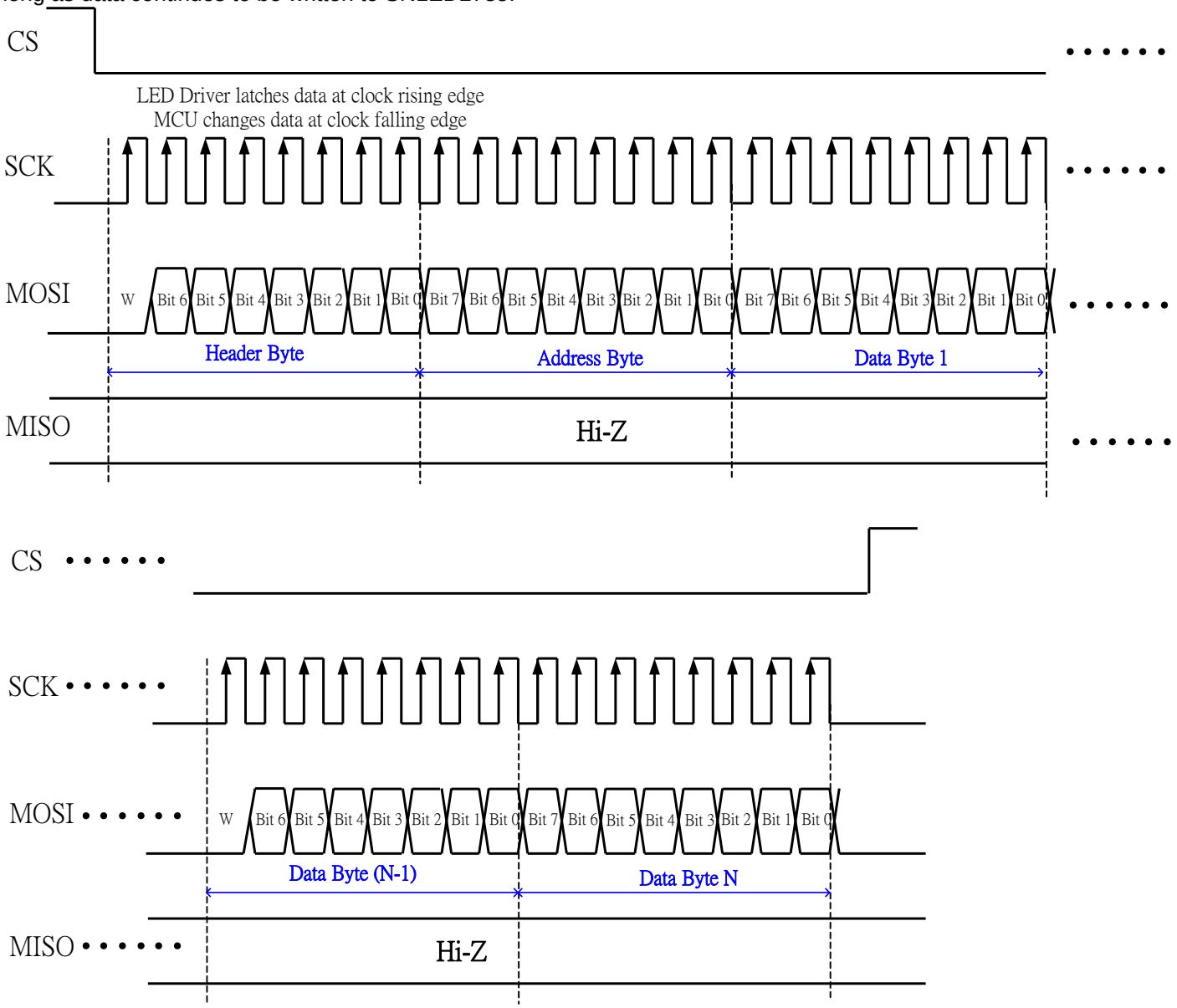
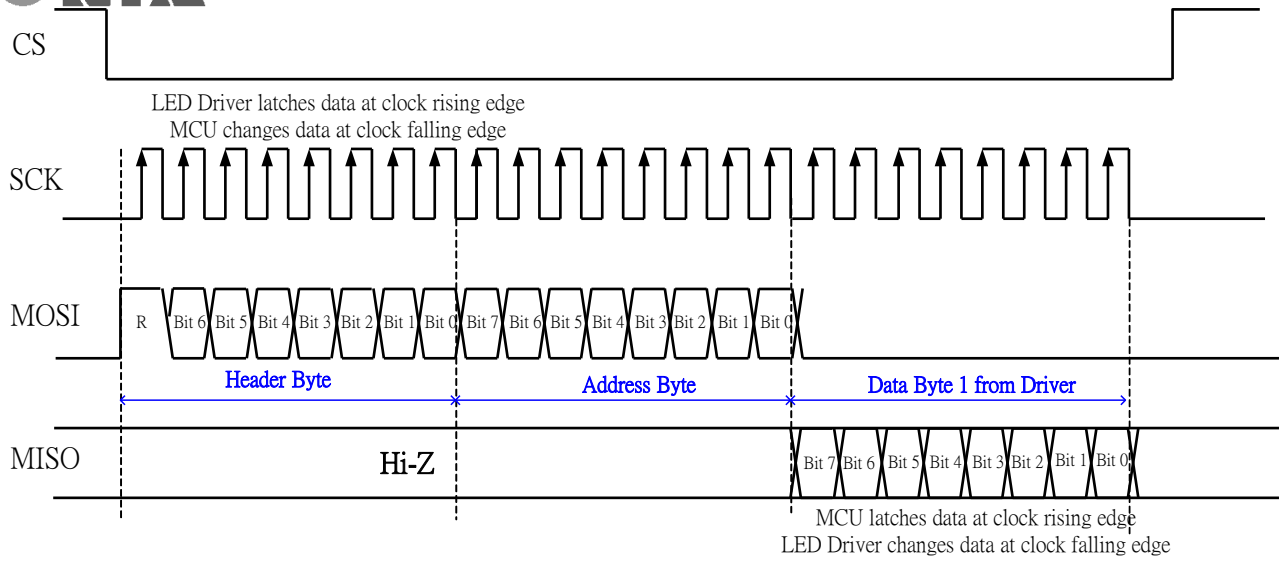


Write to SNLED2735 (Automatic address increment)

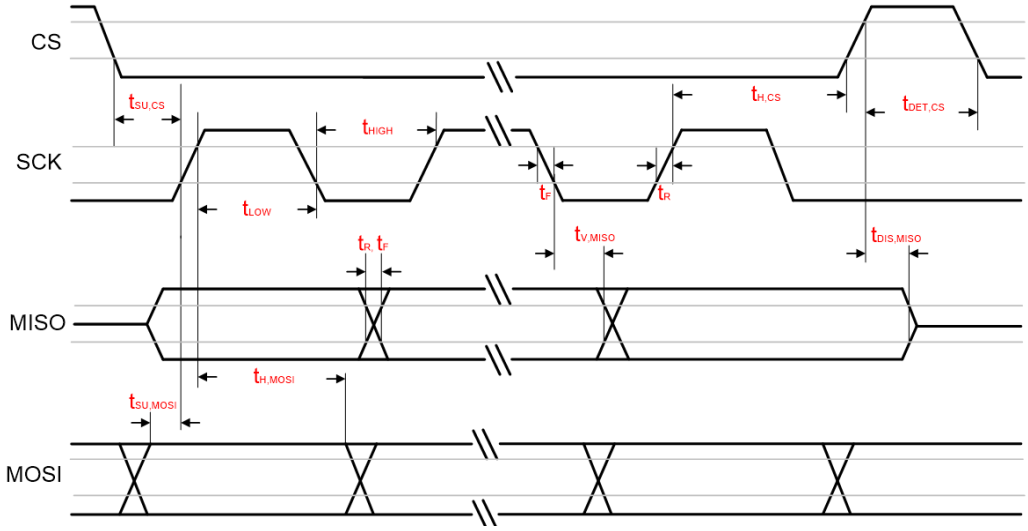
5.2 READING REGISTERS

All of registers in SNLED2735 can be read. But frame Registers can only be read in software shutdown mode as SDB pin high. The Function Register and the Detection Register can be read in software shutdown mode or normal operating mode.

To read the device data, the bus master must first send the SNLED2735 header byte with R/W bit set to “1”, checking pattern and the Response Register, and then send the Address Byte. SNLED2735 will then transmit the data byte addressed by the Address Byte to MCU.



Read from SNLED2735



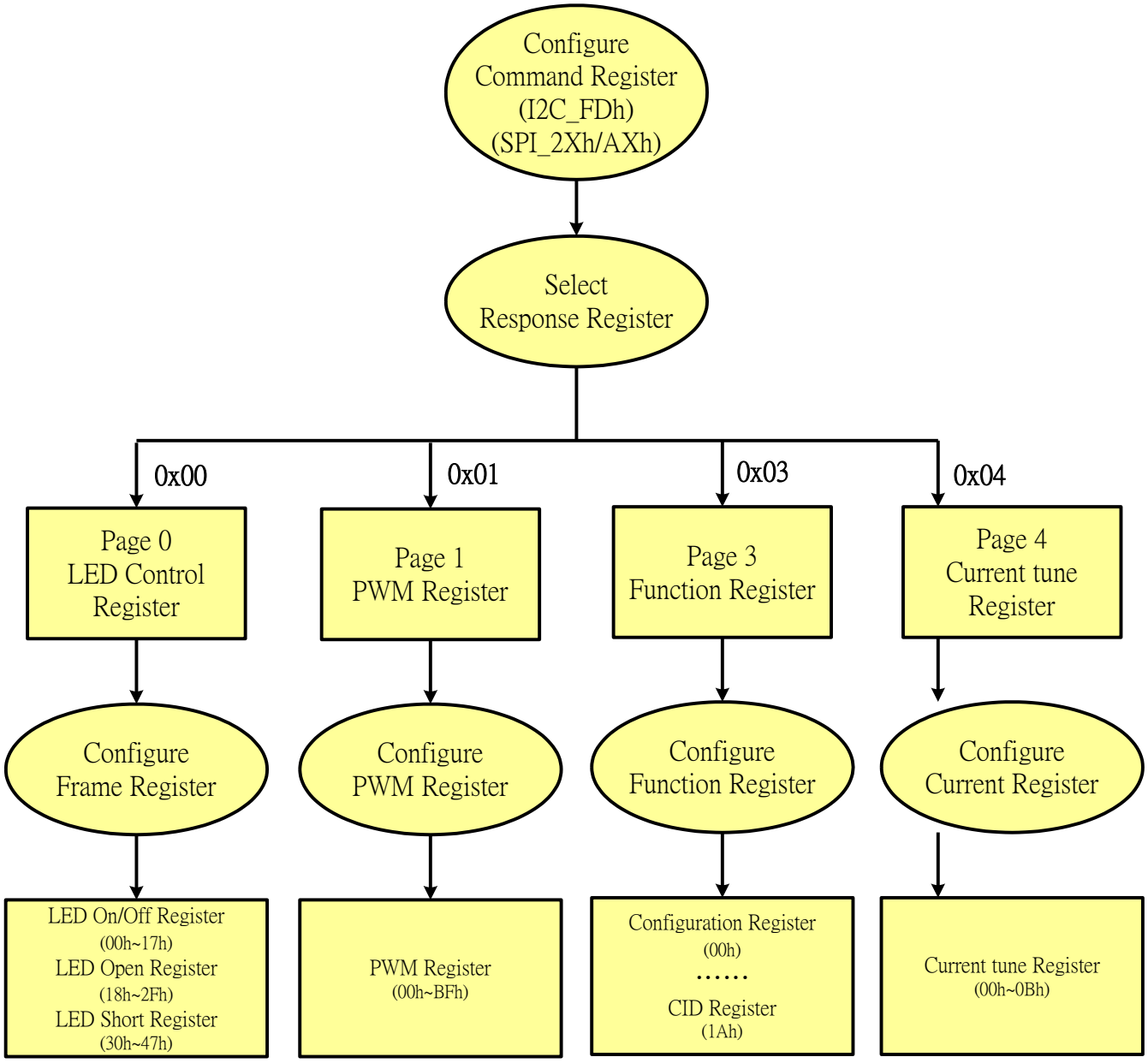
Symbol	Parameter	Min.	Typ.	Max.	Units
f_{SCK}	SPI clock frequency	-	-	4	MHz
t_R	SCK clock Rise time.		7		ns
t_F	SCK clock Fall time.		7		ns
$t_{DET, CS}$	CS detect time	250ns			ns
$t_{SU, CS}$	CS setup time	157ns			ns
$t_{H, CS}$	CS hold time	250ns			ns
t_{LOW}	SCK clock low period.	125ns	-	-	ns
t_{HIGH}	SCK clock high period.	125ns	-	-	ns
$t_{SU, MOSI}$	Data input setup time	31.25ns	-	-	ns
$t_{H, MOSI}$	Data input hold time	125ns	-	-	ns
$t_{DIS, MISO}$	Data output disable time		-	125ns	ns
$t_{V, MISO}$	Data output valid time		-	125ns	ns

6 REGISTER DEFINITION

6.1 REGISTER CONTROL

SNLED2735 support I2C and SPI modes.

In I2C mode, user has to first configure the Command Register (FDh) with the following data 0x00, 0x01, 0x03 or 0x04 to select the Page No.
In SPI mode, SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit (010b) checking pattern bit and 4-bit page bit (0x00, 0x01, 0x03 or 0x04), and then to configure the available registers in that Page No.



6.2 COMMAND REGISTER

Data	Function
0x00	Point to Page 0 (LED Control Register is available)
0x01	Point to Page 1 (PWM Register is available)
0x03	Point to Page 3 (Function Register is available)
0x04	Point to Page 4 (Current Tune Register is available)

6.3 FUNCTION REGISTER TABLE

Address	Name	Function	R/W	Default
LED Control Register (Page 0)				
00h~17h	LED Control Register	Store on or off state for each LED	R/W	0000 0000b
18h~2Fh	LED Open Register	LED Open status for each LED	R	
30h~47h	LED Short Register	LED Short status for each LED	R	
PWM Register (Page 1)				
00h~BFh	PWM Register	192 LEDs PWM duty cycle data register	R/W	0000 0000b
Function Register (Page 3)				
00h	Software Shut Down Register	Set software shutdown mode	R/W	0000 0000b
11h	ID Register	LED Driver ID Register	R	1000 1010b
12h	Thermal Register	Thermal Detector Flag	R/W	0000 0000b
13h	PDU Register	Pull-down and pull-up resistor for LED channel	R/W	
14h	Scan Phase Register	Number of scan phase in one frame.	R/W	
15h	Slew Rate Control Mode1 Register	PWM delay phase setting	R/W	
16h	Slew Rate Control Mode2 Register	Slew rate of current driving and sink IO	R/W	
17h	Open Short Enable Register	Open Short Detect Enable	R/W	
18h	Open Short Duty Register	Open Short Detect Duty	R/W	
19h	Open Short Flag Register	Open Short Detect Flag	R/W	
1Ah	Software Sleep Register	Set software sleep mode	R/W	
Constant Current Step Register (Page 4)				
00h~0Bh	Constant Current Step Register	CB1~CB12 constant current step register	R/W	1100 1100b

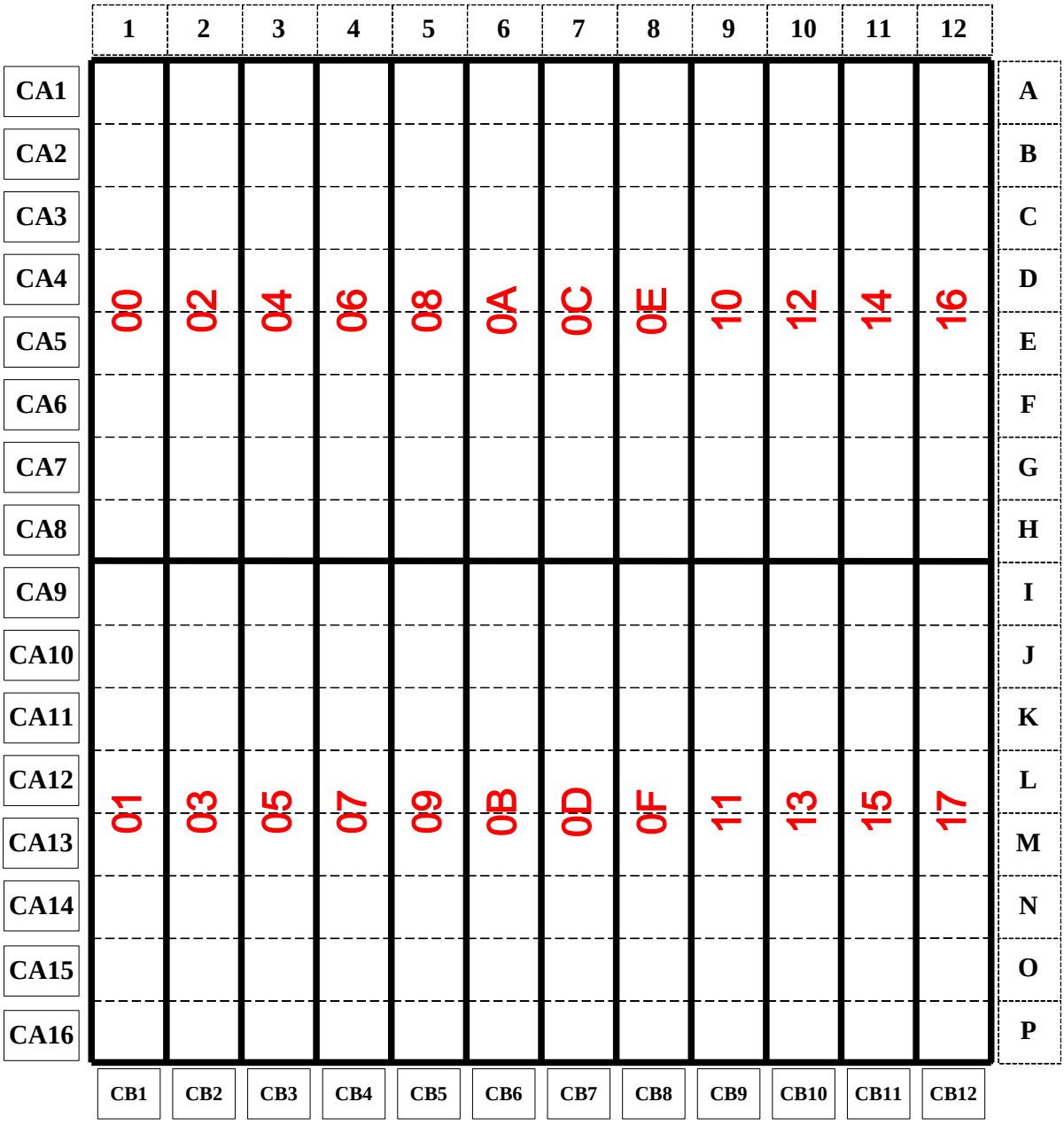
6.4 (PAGE 0) LED CONTROL REGISTER

00h~17h	Bit 7:0
LED Control Register	LED_CTRL
Read/Write	R/W
After Reset	0000 0000b

LED Control Register Address: 00h ~ 17h

The detail ordering of C_{X-Y} can be referred to Memory Map.

C_{X-Y}	LED State Bit
0	LED off
1	LED on



6.5 (PAGE 0) LED OPEN REGISTER

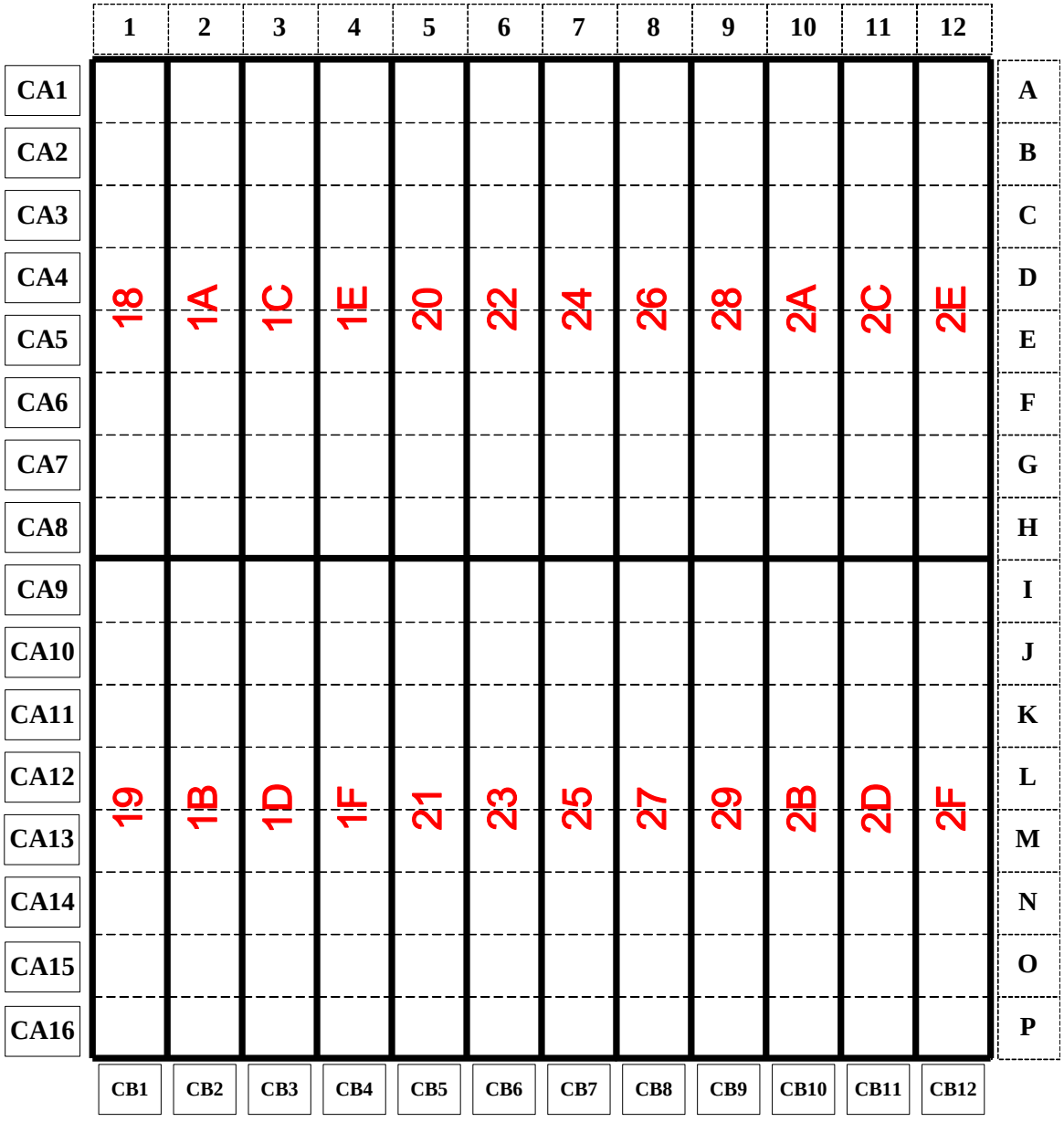
18h~2Fh	Bit 7:0
LED Open Register	**LED_OPEN**
Read/Write	R
After Reset	0000 0000b

LED Open Register Address: 18h ~ 2Fh

The LED Open Registers store the LED open test result of each LED in the 16*12 LED matrix.

C_{X-Y}	LED Open State
0	This LED is detected as 'not OPEN'.
1	This LED is detected as 'OPEN'.

Note: LED is detected as 'OPEN' state when the detected constant current output voltage at M-PWM IO is over VDD – 0.5V. And it is only valid if the corresponding bit in LED Control Register is set as '1'.



6.6 (PAGE 0) LED SHORT REGISTER

30h~47h	Bit 7:0
LED Short Register	LED_SHORT
Read/Write	R
After Reset	0000 0000b

LED Short Register Address: 30h ~ 47h

The LED Short Registers store the LED short test result of each LED in the 16*12 LED matrix.

C_{X-Y}	LED_SHORT State Bit
0	This LED is detected as 'not SHORT'.
1	This LED is detected as 'SHORT'.

Note: LED is detected as 'SHORT' state when the detected constant current output voltage at M-PWM IO is under VSS + 0.5V. And it is only valid if the corresponding bit in LED Control Register is set as '1'.

	1	2	3	4	5	6	7	8	9	10	11	12	
CA1													A
CA2													B
CA3													C
CA4	30	32	34	36	38	3A	3C	3E	40	42	44	46	D
CA5													E
CA6													F
CA7													G
CA8													H
CA9													I
CA10													J
CA11													K
CA12	31	33	35	37	39	3B	3D	3F	41	43	45	47	L
CA13													M
CA14													N
CA15													O
CA16													P
	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11	CB12	

6.7 (PAGE 1) PWM REGISTER

00h~BFh	Bit 7:0
PWM Register	PWM_DUTY
Read/Write	R/W
After Reset	0000 0000b

PWM Register Address: 00h ~ BFh

PWM Registers modulate the 192 LEDs in 255steps.
PWM_DUTY: 00h ~ FFh

	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11	CB12	
	0	1	2	3	4	5	6	7	8	9	A	B	
CA1	00	10	20	30	40	50	60	70	80	90	A0	B0	0
CA2	01	11	21	31	41	51	61	71	81	91	A1	B1	1
CA3	02	12	22	32	42	52	62	72	82	92	A2	B2	2
CA4	03	13	23	33	43	53	63	73	83	93	A3	B3	3
CA5	04	14	24	34	44	54	64	74	84	94	A4	B4	4
CA6	05	15	25	35	45	55	65	75	85	95	A5	B5	5
CA7	06	16	26	36	46	56	66	76	86	96	A6	B6	6
CA8	07	17	27	37	47	57	67	77	87	97	A7	B7	7
CA9	08	18	28	38	48	58	68	78	88	98	A8	B8	8
CA10	09	19	29	39	49	59	69	79	89	99	A9	B9	9
CA11	0A	1A	2A	3A	4A	5A	6A	7A	8A	9A	AA	BA	A
CA12	0B	1B	2B	3B	4B	5B	6B	7B	8B	9B	AB	BB	B
CA13	0C	1C	2C	3C	4C	5C	6C	7C	8C	9C	AC	BC	C
CA14	0D	1D	2D	3D	4D	5D	6D	7D	8D	9D	AD	BD	D
CA15	0E	1E	2E	3E	4E	5E	6E	7E	8E	9E	AE	BE	E
CA16	0F	1F	2F	3F	4F	5F	6F	7F	8F	9F	AF	BF	F

6.8 (PAGE 3) FUNCTION REGISTER

00h	Bit 7:1	Bit 0
Software Shut Down Register	**-**	**SSD**
Read/Write	R	R/W
After Reset	0000 000b	0b

The SSD Register sets software shutdown mode.

SSD	**Software Shutdown Control**
0	SW Shutdown Mode.
1	Normal Mode.

11h	Bit 7:0
ID Register	**ID**
Read/Write	R
After Reset	1000 1010b

Read the LED Driver ID register to confirm the system in operation mode.

ID **LED Driver ID Register**

12h	Bit 7:1	Bit 0
Thermal Register	-	**TDF**
Read/Write	R	R
After Reset	0000 000b	0b

Read the TDF register to monitor the system temperature.

TDF	**Thermal detect Flag**
0	System temperature is under 70°C.
1	System temperature reaches or is over 70°C.

13h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDU Register	**CAPD**	-	**CAPD2**	**-**	**CBPU**	-	**CBPU2**	-
Read/Write	R/W	R	R/W	R	R/W	R	R/W	R
After Reset	0b	0b	0b	0b	0b	0b	0b	0b

Setting pull-down resistor for CA1~CA16 and pull-up resistor for CB1~CB12.

CAPD **Pull-down control bit for CA1~CA16 on latch data time.**
0 Floating on latch data time.
1 Enable pull- down for CA1~CA16 on latch data time.

CAPD2 **Pull-down control bit for CA1~CA16 on Scan time.**
0 Floating on Scan (PWM off) time.
1 Enable pull- down for CA1~CA16 on Scan (PWM off) time.

CBPU **Pull-up control bit for CB1~CB12 on latch data time.**
0 Floating.
1 Enable pull- up for CB1~CB12 on latch data time.

CBPU2 **Pull-up control bit for CB1~CB12 on scan time.**
0 Floating.
1 Enable pull- up for CB1~CB12 on not scan channel (scan time).

14h	Bit 7:4	Bit 3:0
Scan Phase Register	-	**SP**
Read/Write	R	R/W
After Reset	0000b	0000b

Setting number of scan phase in one frame.

SP **Scan Phase Setting**
0000 Scan phase is CB1 ~ CB12, 1/12.
0001 Scan phase is CB1 ~ CB11, 1/11, CB12 no-active.
0010 Scan phase is CB1 ~ CB10, 1/10, CB11~CB12 no-active.
0011 Scan phase is CB1 ~ CB9, 1/9, CB10~CB12 no-active.
0100 Scan phase is CB1 ~ CB8, 1/8, CB9~CB12 no-active.
0101 Scan phase is CB1 ~ CB7, 1/7, CB8~CB12 no-active.
0110 Scan phase is CB1 ~ CB6, 1/6, CB7~CB12 no-active.
0111 Scan phase is CB1 ~ CB5, 1/5, CB6~CB12 no-active.
1000 Scan phase is CB1 ~ CB4, 1/4, CB5~CB12 no-active.
1001 Scan phase is CB1 ~ CB3, 1/3, CB4~CB12 no-active.
1010 Scan phase is CB1 ~ CB2, 1/2, CB3~CB12 no-active.
1011 Scan phase is only CB1, 1/1, CB2~CB12 no-active.

15h	Bit 7:3	Bit 2	Bit 1:0
Slew Rate Control Mode1 Register	-	**PDP_EN**	-
Read/Write	R/W	R/W	R/W
After Reset	0000 0b	0b	00b

The Slew Rate Control Register Mode1 sets the delay phase of PWM.

PDP_EN **PWM Delay Phase enable**
0 Delay phase disable.
1 Delay phase enable.

Note: Slew Rate Control Mode1 register need setting 0x00 or 0x04.

16h	Bit 7	Bit 6	Bit 5:0
Slew Rate Control Mode2 Register	**DSL**	**SSL**	**-**
Read/Write	R/W	R/W	R
After Reset	0b	0b	00 0000b

The Slew Rate Control Mode2 Register sets the slew rate of current source and sink IO.

DSL **Driving Channel Slew Rate Enable.**
0 Disable.
1 Enable.
SSL **Sinking Channel Slew Rate Enable.**

0 Disable.
1 Enable.

17h	Bit 7	Bit 6	Bit 5:0
Open Short Enable Register	**ODS**	**SDS**	**-**
Read/Write	W	W	R
After Reset	0b	0b	00 0000b

The Open Short Enable Register is used to enable the open/short detection test.

ODS **Open Detection Start**
0 Not enable open detection test. (H/W clear automatically)
1 Start open detection test.

SDS **Short Detection Start**
0 Not enable short detection test. (H/W clear automatically)
1 Start short detection test.

18h	Bit 7:0
Open Short Duty Register	**OSDD**
Read/Write	R/W
After Reset	0000 0000b

The Open Short Duty Register is latched duty.
OSDD **Open Short Detection Duty**
The PWM duty that Open Short detection is latched.
The latched duty 0 is reserved, and the usable duty ranges from 0x01~0xFA.
For example, when OSDD is 16, the open short latched duty is 16.

Note: Once OSDD is set, all other operation modes are ignored and the system starts to re-run the LED matrix for the LED open short detection. And the OSDD will be cleared as '0' by H/W automatically. After the open short detection has completed scanning the full LED matrix, the OSDINT will be set as '1' by H/W automatically.

Note: To do open short detection or not depends on the LED Control Register setting. Any bit set as '0' in LED Control Register means no open short detection will run at that corresponding LED location. Also, the corresponding bit in LED Open Register and LED Short Register will be always set as '0' after open short detection is completed.

19h	Bit 7	Bit 6	Bit 5:0
Open Short Flag Register	**ODINT**	**SDINT**	**-**
Read/Write	R/W	R/W	R
After Reset	0b	0b	00 0000b

The Open Short Flag Register is used to indicate the open/short detection status.

ODINT **Open Detection Interrupt**
0 Open detection test is not completed.
1 Open detection test is completed. (H/W set automatically)

SDINT **Short Detection Interrupt**
0 Short detection test is not completed.
1 Short detection test is completed. (H/W set automatically)

1Ah	Bit 7:2	Bit 1	Bit 0
Software Sleep Register	**-**	**SLEEP**	**IREF_EN**
Read/Write	R	W	R/W
After Reset	0000 00b	0b	0b

The Software Sleep Register sets sleep mode.

SLEEP	**Software Sleep Control.**
0	Disable Sleep Mode.
1	Enable Sleep Mode. (Wakeup clear automatically)

Note: Sleep mode wakeup source are SDB pin, SYSRST pin or SCL/SCK pin level change.

The IREF_EN register sets the internal setting function.

IREF_EN	**IREF mode.**
0	Disable IREF Mode.
1	Enable IREF Mode.

Note: IREF mode need to set as “0”.

6.9 (PAGE 4) CURRENT TUNE REGISTER

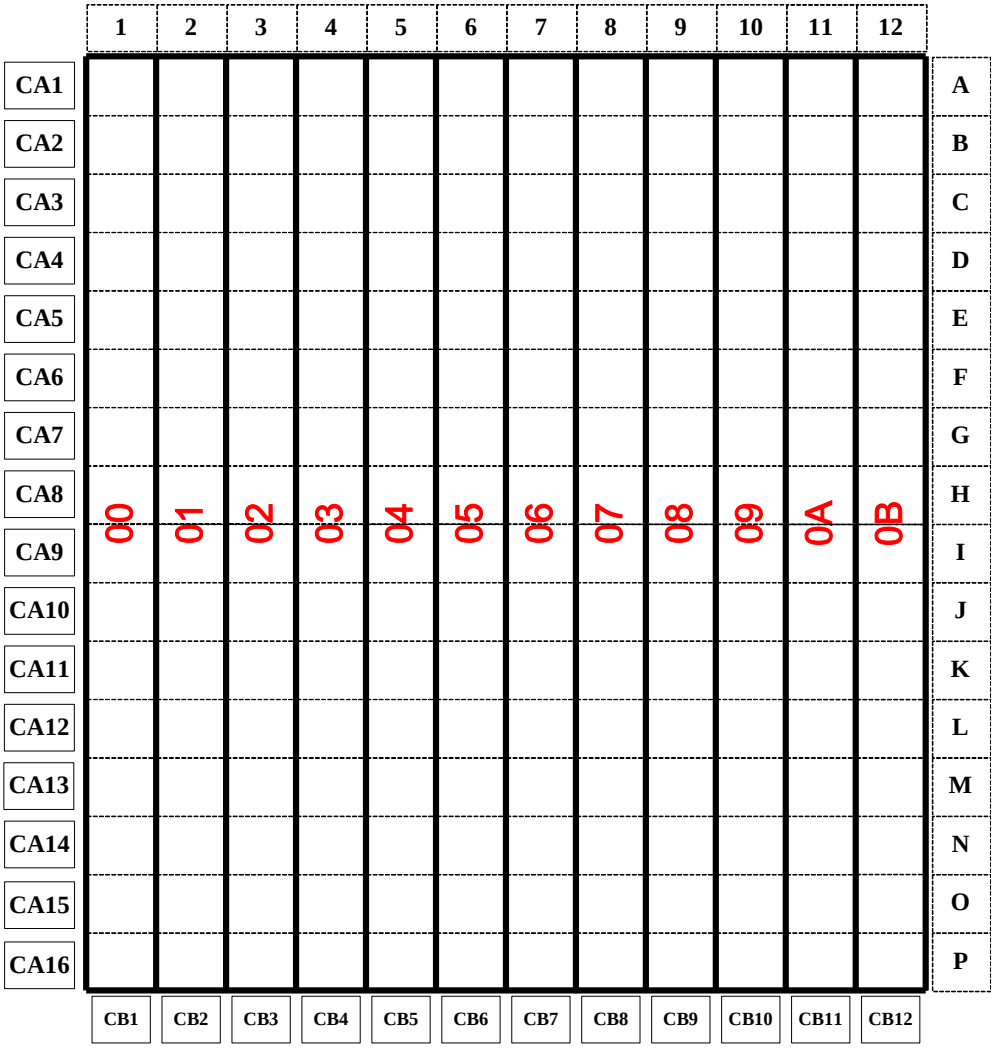
00h~0Bh	Bit 7:0
Constant Current Step Register	**CCS**
Read/Write	R/W
After Reset	1100 1100b

The Constant Current Step register sets the constant current of the CB1~CB12 channel.

CCS **CB1~CB12 channel Constant Current Step**

If CCS = 0, constant current control is disabled. The output current I_{out} is 0mA.
If CCS = 1~3, constant source current I_{out} is 0.47mA.
If CCS = 4~255, constant source current I_{out} is [Constant Current Step x 0.157] mA.

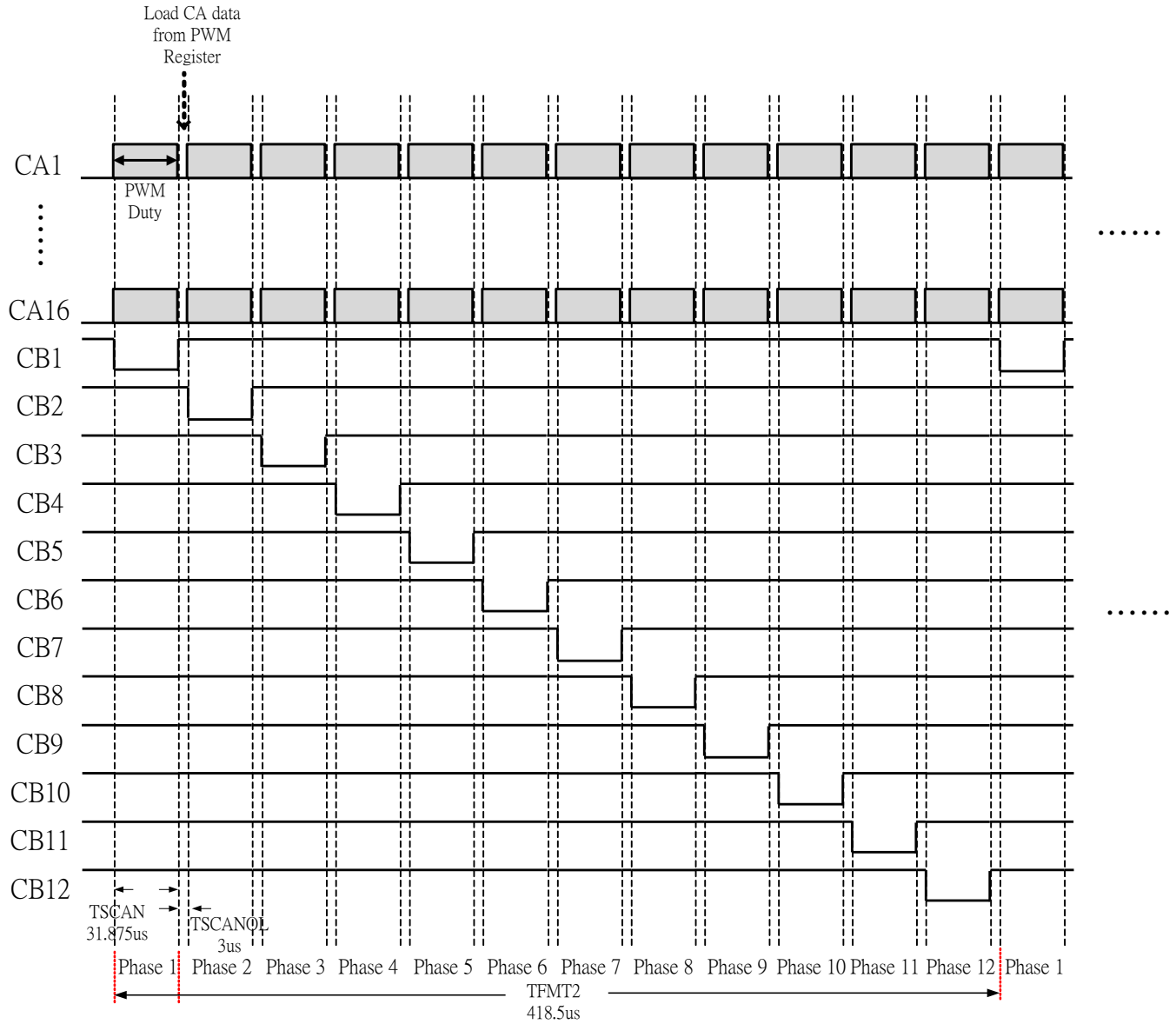
For example:
when CCS = 204, Iout is [204*0.157] = 32mA



Note: Please reference Scan Phase Register to setting Constant Current Step register.

7 PHASE MECHANISM

7.1 PHASE TIME



The LED scan time $\mathbf{T_{SCAN}}$ = 255 x $\mathbf{T_{MCLK}}$ = 255 x (8MHz) = 31.875us.

The blanking time $\mathbf{T_{SCANOL}}$ = 24 x $\mathbf{T_{MCLK}}$ = 24 x (8MHz) = 3us.

For matrix, $\mathbf{T_{FMT2}}$ = Phase No. x (T_{SCAN} + T_{SCANOL}) = 12 x (31.875us + 3us) = 418.5us

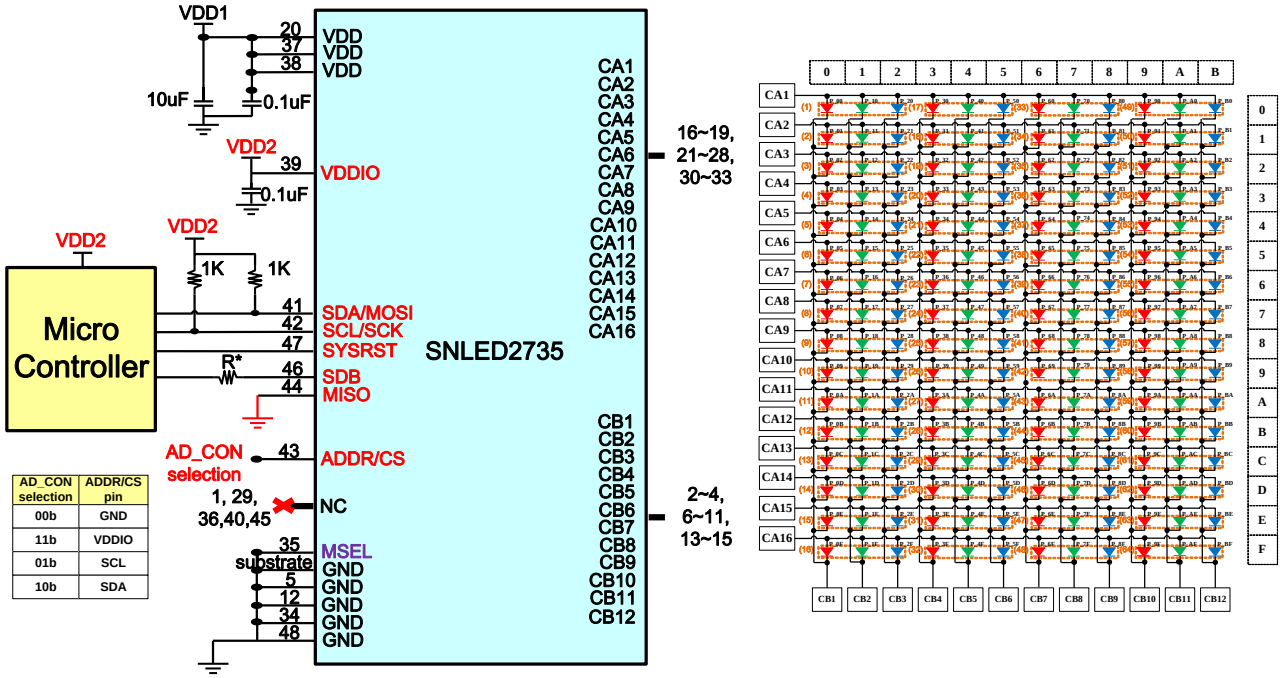
PWM frequency $\mathbf{F_{PWM}}$ = 1 / 34.875us = 28.7KHz

Note: Slew Rate Control Mode1 register sets 0x00 to disable PWM Delay Phase setting.

8 APPLICATION CIRCUIT

8.1 SNLED2735 INTERFACE WITH LED MATRIX

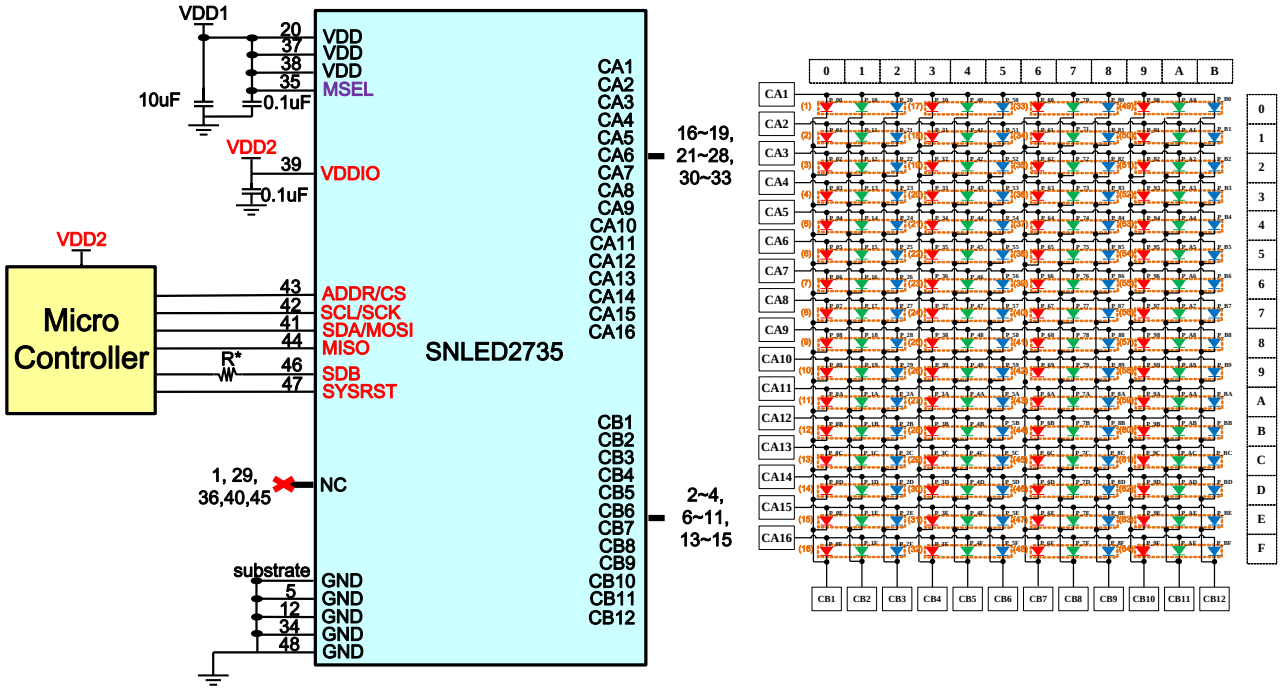
I2C INTERFACE



AD_CON selection	ADDR/CS pin
00b	GND
11b	VDDIO
01b	SCL
10b	SDA

NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

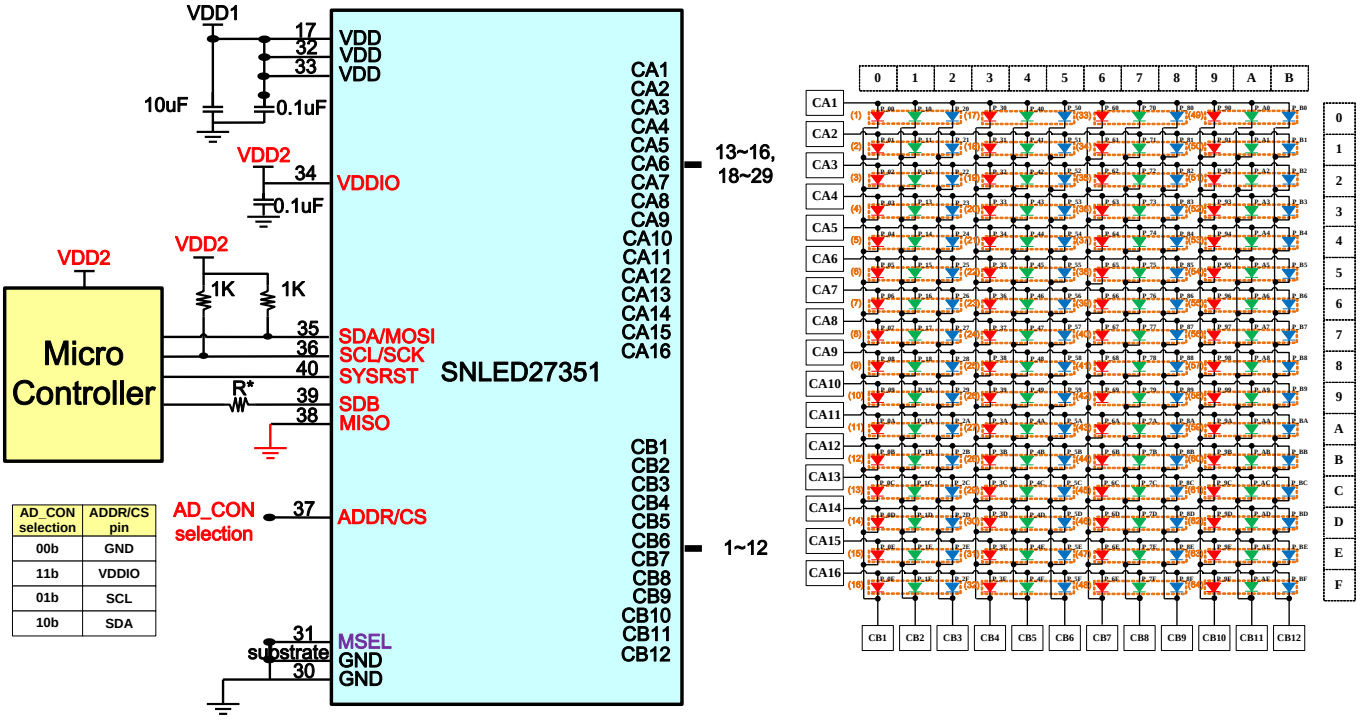
SPI INTERFACE



NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

8.2 SNLED27351 INTERFACE WITH LED MATRIX

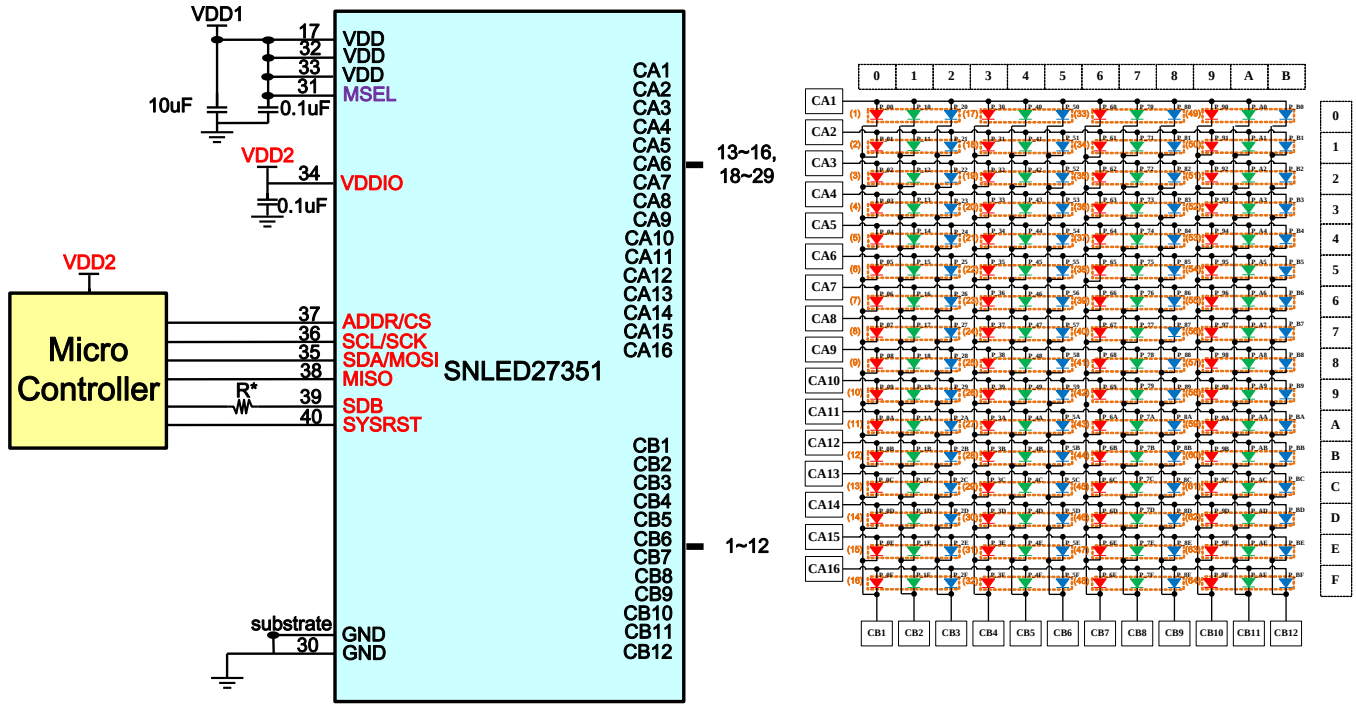
8.2.1 I2C INTERFACE



AD_CON selection	ADDR/CS pin
00b	GND
11b	VDDIO
01b	SCL
10b	SDA

NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

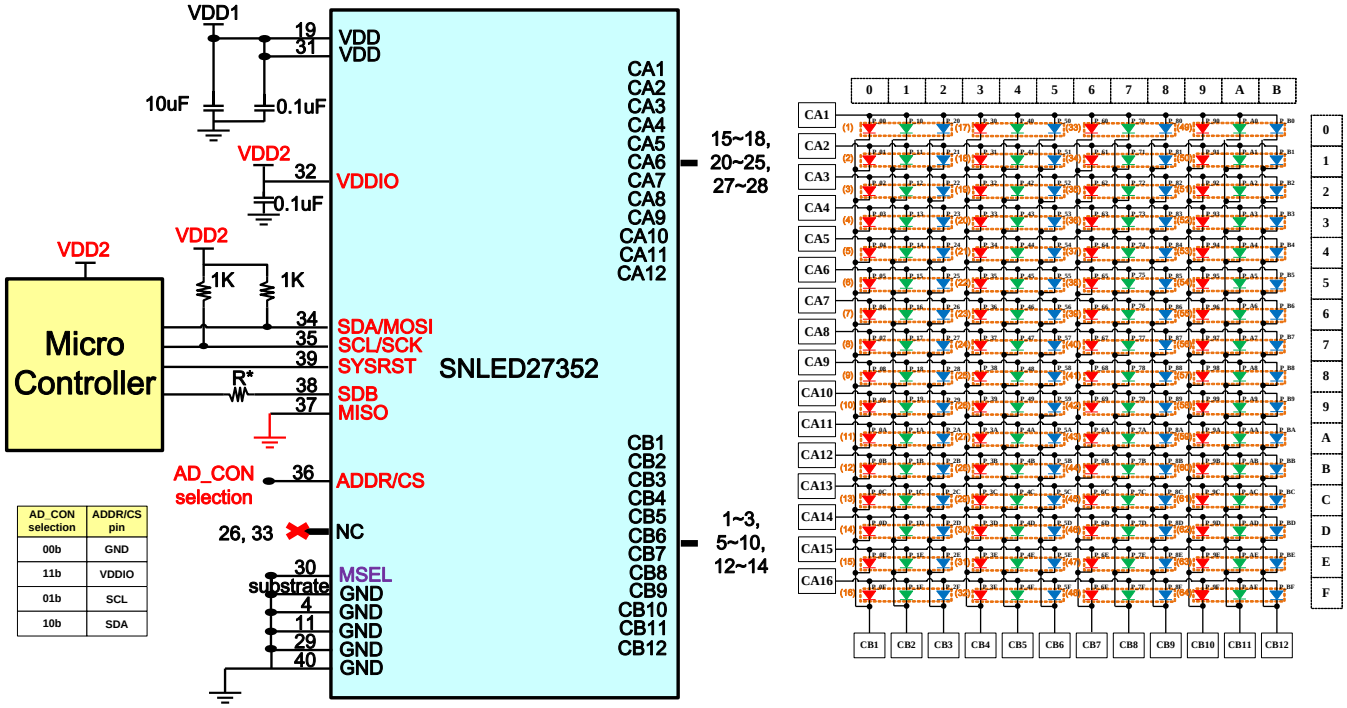
8.2.2 SPI INTERFACE



NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

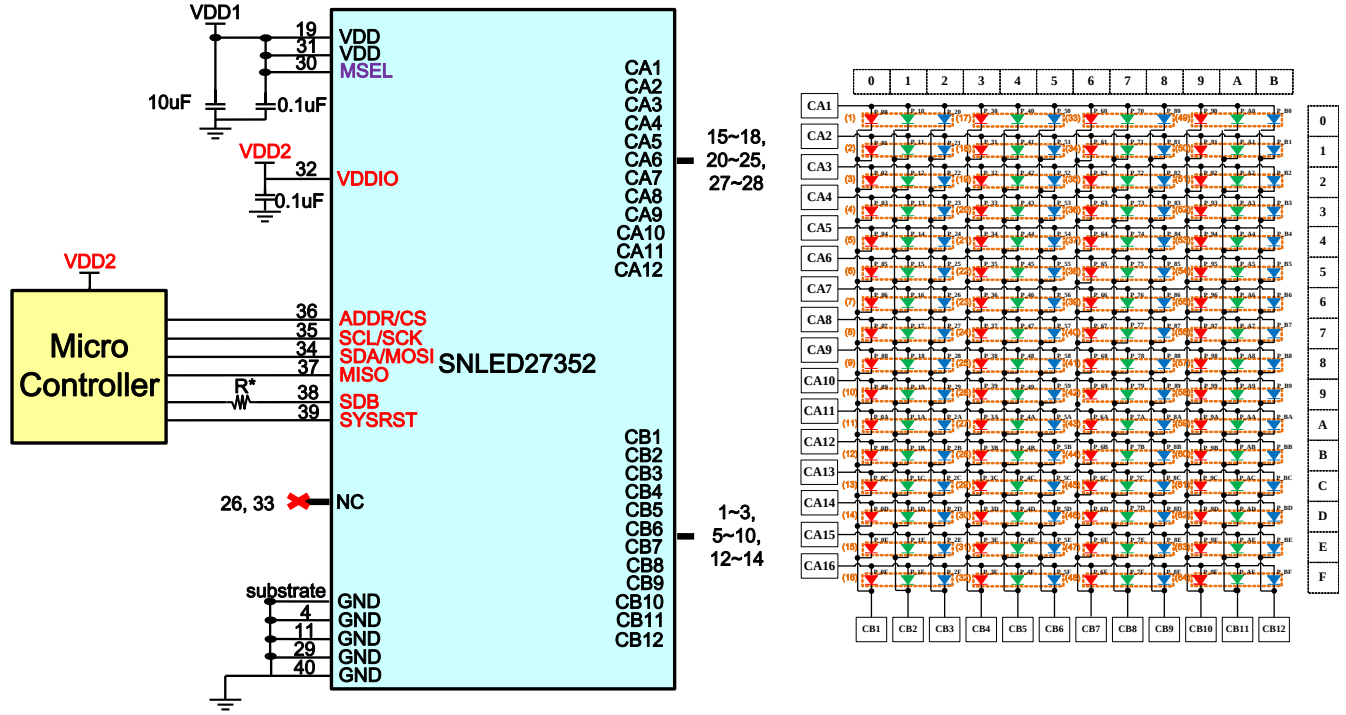
8.3 SNLED27352 INTERFACE WITH LED MATRIX

8.3.1 I2C INTERFACE



NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

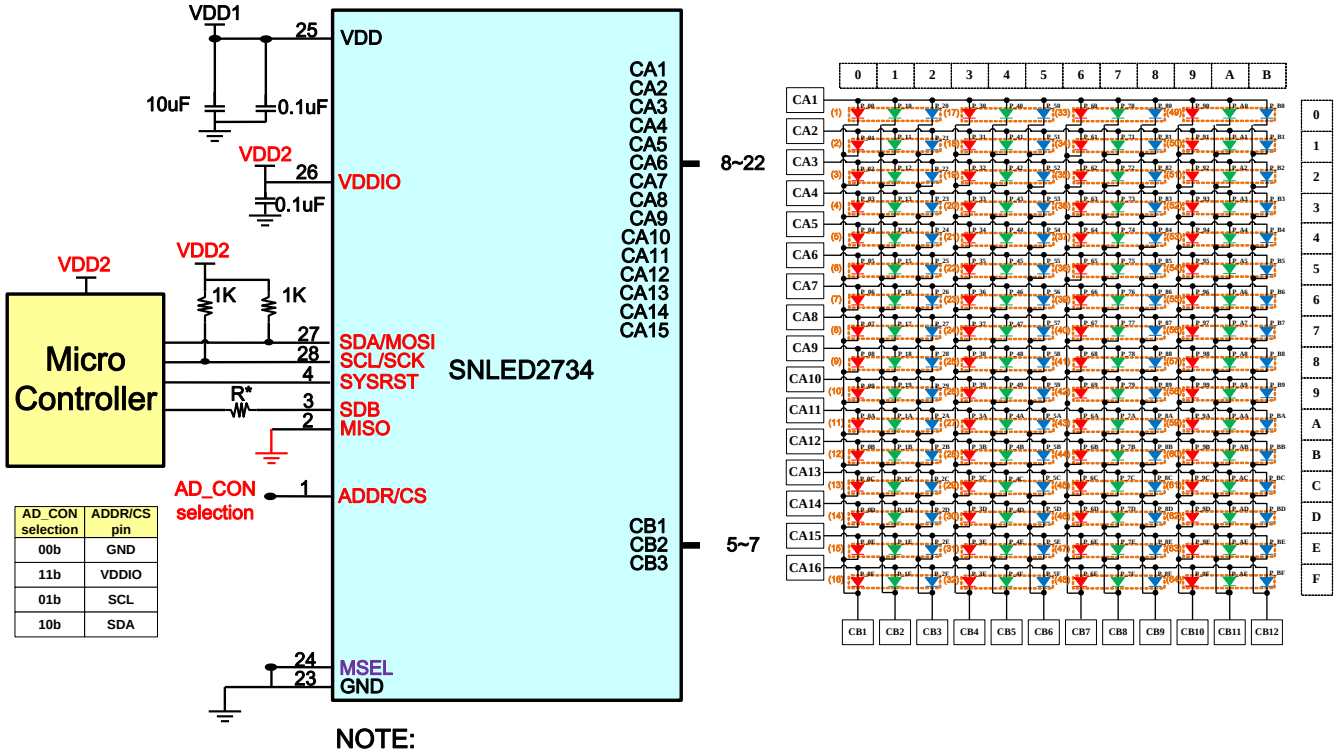
8.3.2 SPI INTERFACE



NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

8.4 SNLED2734 INTERFACE WITH LED MATRIX

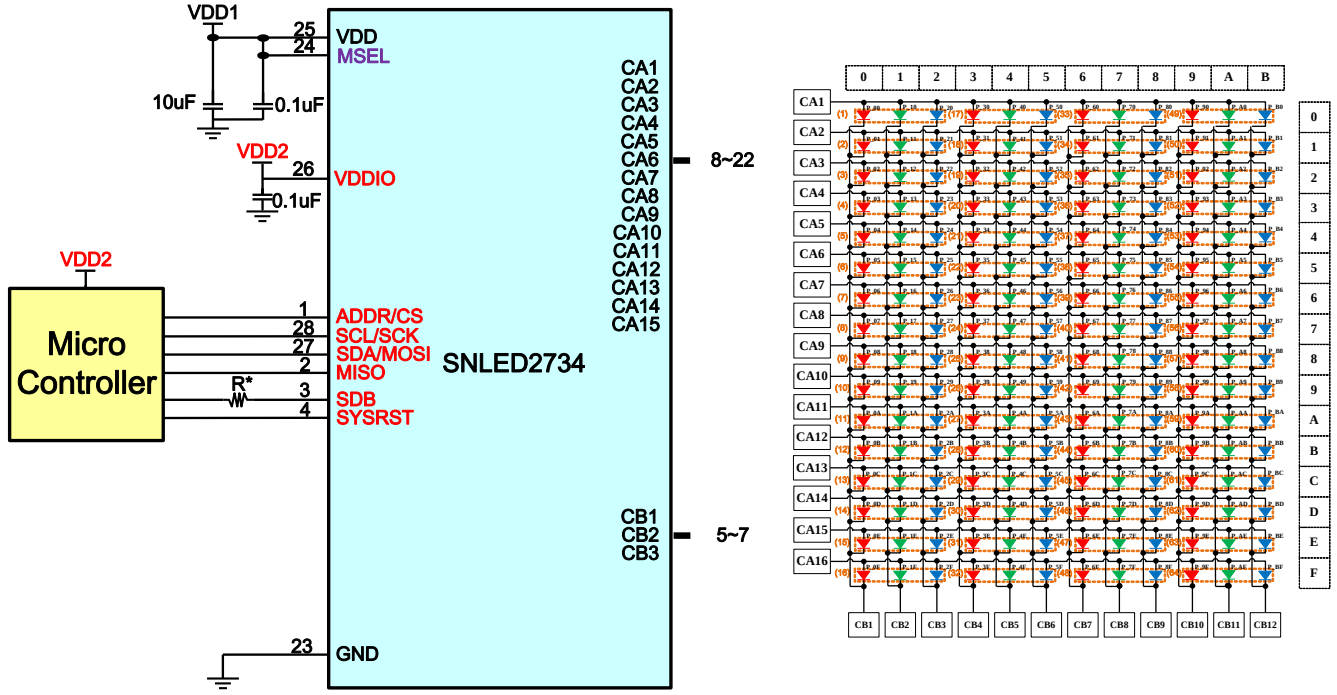
8.4.1 I2C INTERFACE



AD_CON selection	ADDR/CS pin
00b	GND
11b	VDDIO
01b	SCL
10b	SDA

NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

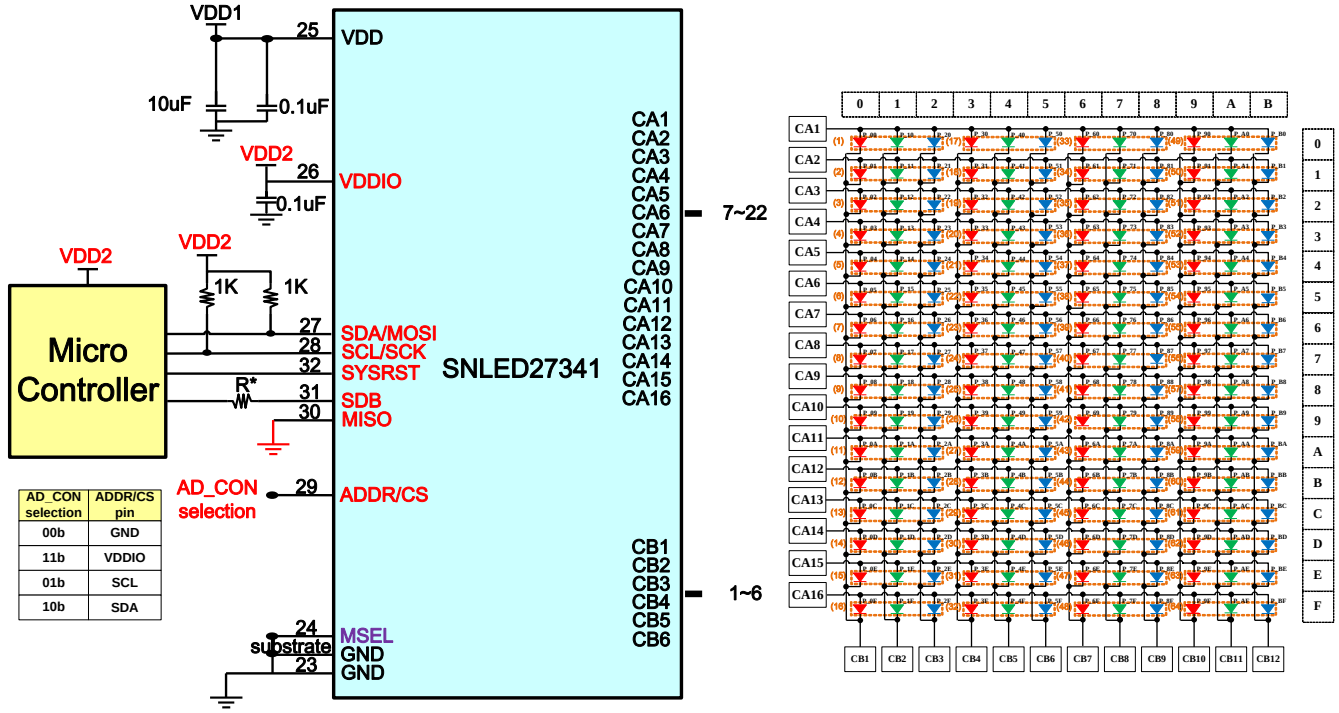
8.4.2 SPI INTERFACE



NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

8.5 SNLED27341 INTERFACE WITH LED MATRIX

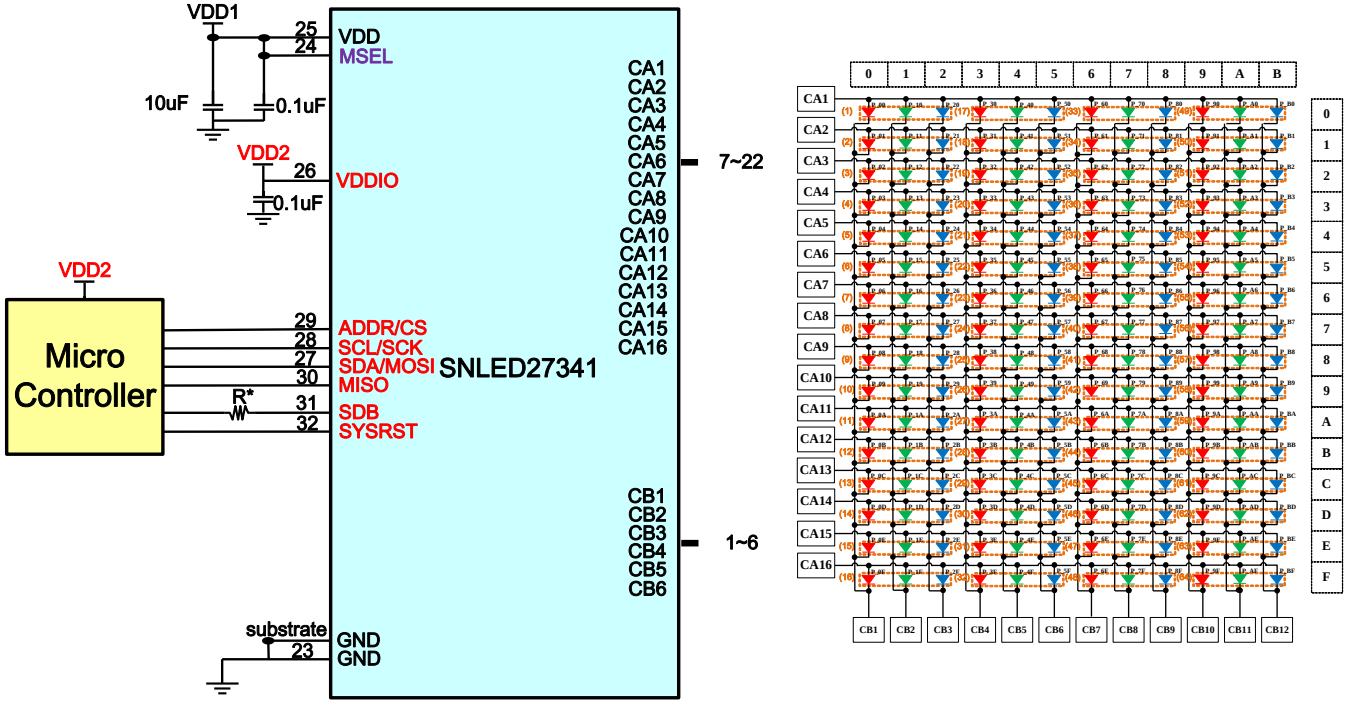
8.5.1 I2C INTERFACE



AD_CON selection	ADDR/CS pin
00b	GND
11b	VDDIO
01b	SCL
10b	SDA

NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

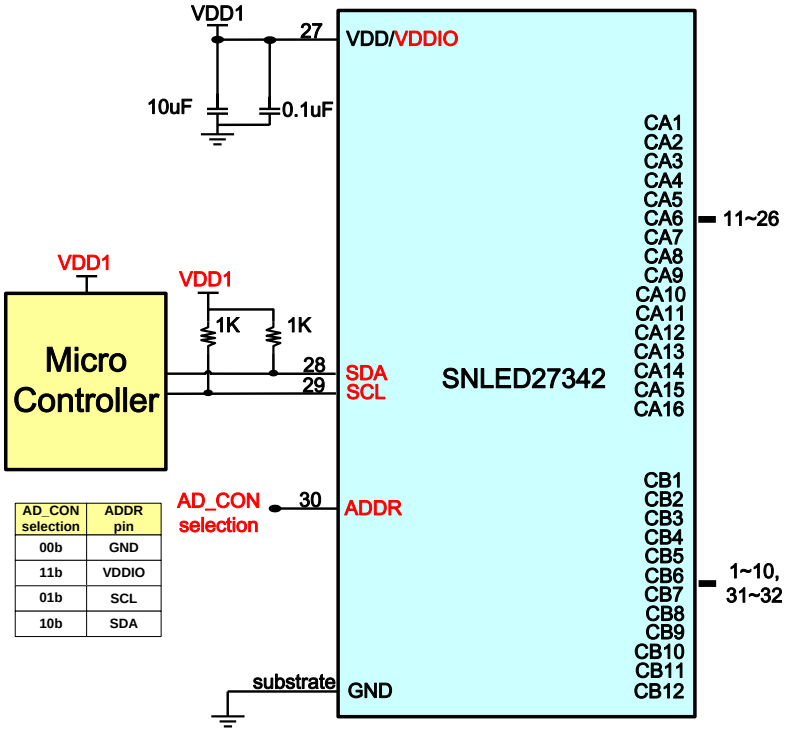
8.5.2 SPI INTERFACE



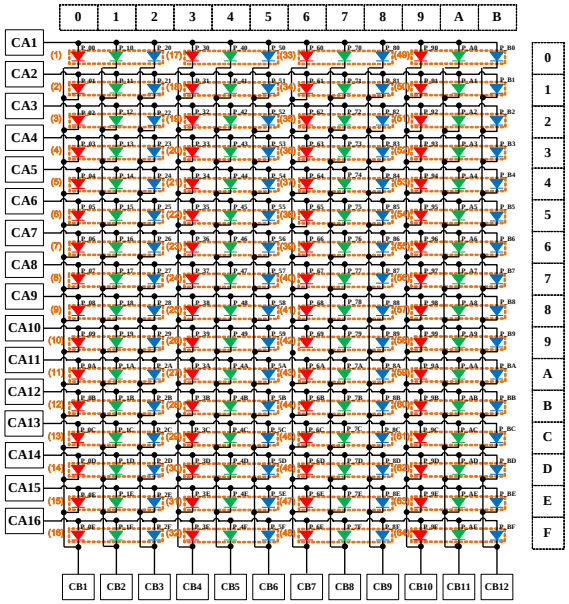
NOTE:
VDDIO = VDD, SDB pin connect R* = 0ohm to MCU.
VDDIO < VDD, SDB pin connect R* = 200Kohm to MCU.

8.6 SNLED27342 INTERFACE WITH LED MATRIX

8.6.1 I2C INTERFACE



AD_CON selection	ADDR pin
00b	GND
11b	VDDIO
01b	SCL
10b	SDA

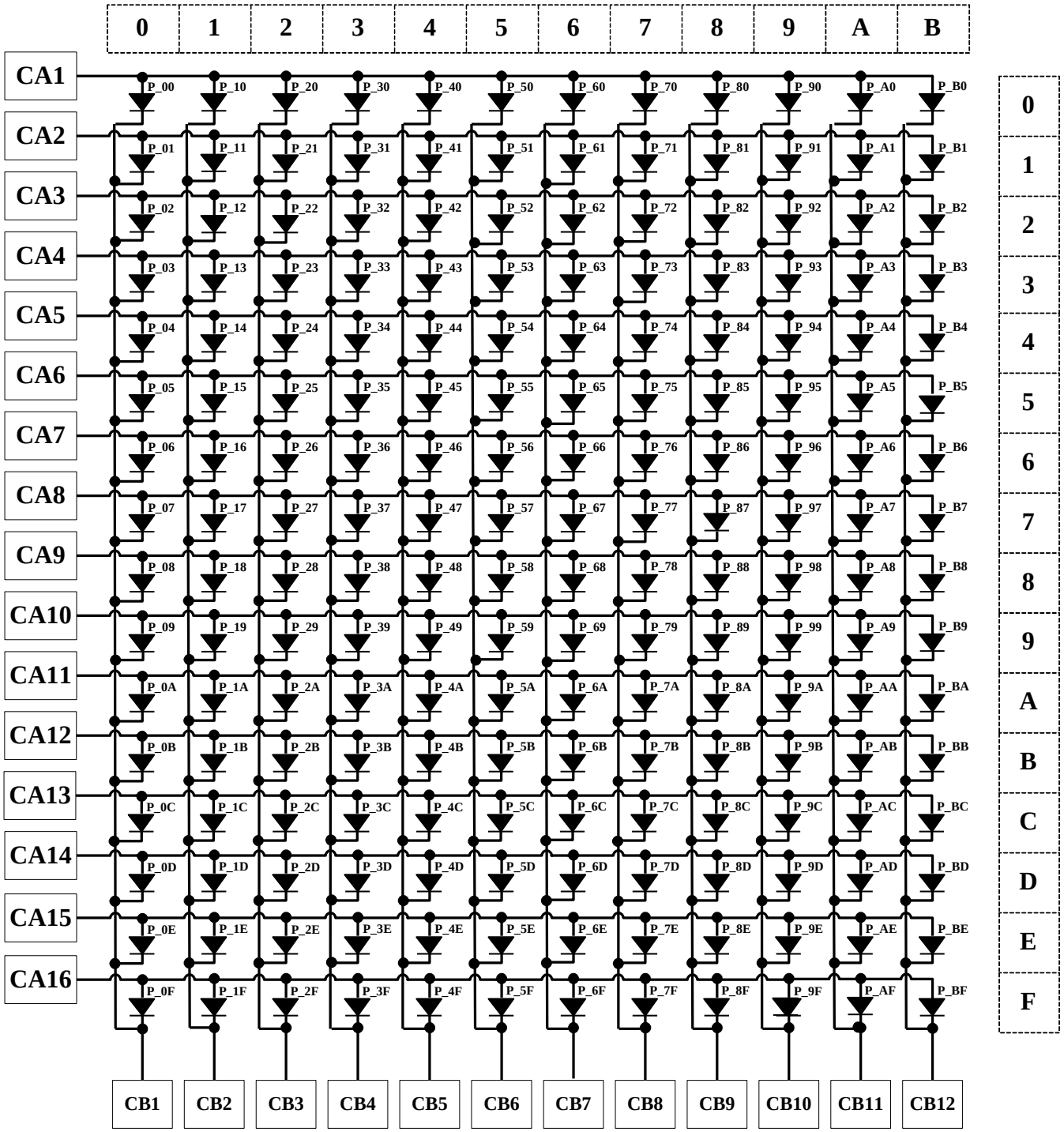


8.7 SNLED2730 RGB LED MATRIX PLACEMENT

8.7.1 SNLED2730 SINGLE COLOR LED IN MATRIX

LED Matrix can drive 192 single color LEDs. The locations of single color LEDs are recommended as the circuit below.

Reference PWM register: (PAGE 1) PWM REGISTER

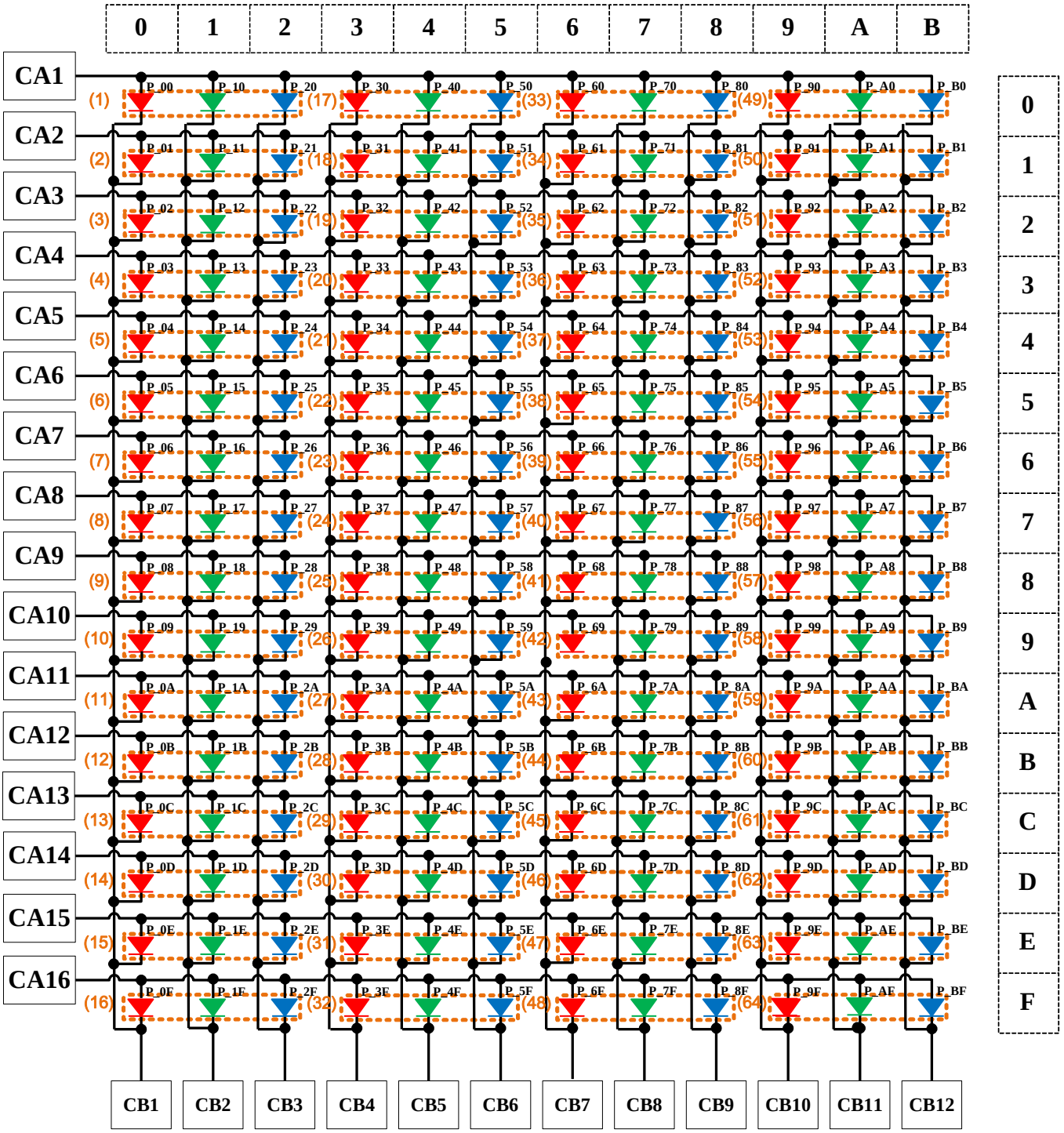


Matrix: 16*12

8.7.2 SNLED2730 COMMON ANODE RGB LED IN MATRIX

LED Matrix can drive 64 common Anode RGB LEDs. The locations of RGB LEDs are recommended as the circuit below.

Reference PWM register: (PAGE 1) PWM REGISTER



Matrix: 16*12

8.8 SNLED2730 SAMPLE CODE

8.8.1 SNLED2730 SETTING IN I2C MODE

➢ Set SNLED2730 Initial Value

```
//=========================================//
// Set LED Driver HW Setting               //
//=========================================//
__LED_SetMSELPinLow                    //** set SNLED2735 to I2C mode
__LED_SetADDRPin                       //** set SNLED2735_ADDRESS
__LED_SetSDBPinHigh;                   //** tie SNLED2735 SDB pin High into normal mode
__Delay(25ms);
__LED_SetRSTPinHigh;                   //** tie SNLED2735 SYSRST pin High to start
__Delay(25ms);
//=========================================//
// Set LED FUNCTION PAGE (Page 3)          //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x03);      //** Select to function page (Page 3)
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x00, 0x00);      //** Setting LED driver to shutdown mode
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x13, 0xAA);      //** Setting internal channel pulldown/pullup
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x14, 0x00);      //** Select scan phase to CB1~CB12
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x15, 0x04);      //** Setting PWM Delay Phase enable
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x16, 0xC0);      //** Setting CA/CB Channel Slew Rate enable
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x1A, 0x00);      //** Setting Iref mode disable
//=========================================//
// Clear LED CONTROL PAGE (Page 0)         //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x00);      //** Select to LED control page (Page 0)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0x47, 0x00);  //** Clear LED Control Register 0x00~0x47 data
//=========================================//
// Clear PWM PAGE (Page 1)                 //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x01);      //** Select to LED control page (Page 1)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0xBF, 0x00);  //** Clear PWM Register 0x00~0xBF data
//=========================================//
// Set CURRENT PAGE (Page 4)               //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x04);      //** Select to LED control page (Page 4)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0x0B, 0x80);  //** Setting CCS Register Addr. 0x00~0x0B = 20mA
```

➢ Switch SNLED2730 LED Effect Algorithm

```
//=========================================//
// Set LED driver to shutdown mode (Page 3)  //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x03);          //** Select to function page (Page 3)
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x00, 0x00);          //** Setting LED driver to shutdown mode
//=========================================//
// Set 192 LEDs Control ON/OFF Register (Page 0)  //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x00);          //** Select to LED control page (Page 0)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0x17, 0xFF);    //** Setting 192 LEDs Control Register ON
//=========================================//
// Set CURRENT PAGE (Page 4)                 //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x04);          //** Select to LED control page (Page 4)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0x0B, 0xCC);    //** Setting CCS Register 0x00~0x0B data to 0xCC
//=========================================//
// Clear PWM PAGE (Page 1)                   //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x01);          //** Select to LED control page (Page 1)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0xBF, 0x00);    //** Clear PWM Register 0x00~0xBF data
//=========================================//
// Setting LED driver to normal mode (Page 3)  //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x03);          //** Select to function page (Page 3)
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x00, 0x01);          //** Setting LED driver to normal mode
```

➢ Set SNLED2730 LED Effect Algorithm

```
//=========================================//
// Set LED PWM Effect Algorithm (Page 1)     //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x01);          //** Select to LED control page (Page 1)
I2C_W_NBYTE(SNLED2735_ADDRESS, 0x00, 0xBF, 0xFF);    //** Setting 192 LEDs PWM Register data to 0xFF
Setting LED Algorithm…
```

➢ Set SNLED2730 to Software Sleep

```
//=========================================//
// Set Software Sleep (Page 3)               //
//=========================================//
I2C_W_2BYTE(SNLED2735_ADDRESS, 0xFD, 0x03);          //** Select to function page (Page 3)
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x00, 0x00);          //** Setting LED driver to shutdown mode
I2C_W_2BYTE(SNLED2735_ADDRESS, 0x1A, 0x02);          //** Setting Software sleep
```

```
__Delay(1ms);
```

8.8.2 SNLED2730 SETTING IN SPI MODE

➢ Set SNLED2730 Initial Value

```
//=========================================//
// Set LED Driver HW Setting                //
//=========================================//
__LED_SetMSELPinHigh                        //** set SNLED2735 to SPI mode
__LED_SetSDBPinHigh;                        //** tie SNLED2735 SDB pin High into normal mode
__Delay(25ms);
__LED_SetRSTPinHigh;                        //** tie SNLED2735 SYSRST pin High to start
__Delay(25ms);
//=========================================//
// Set LED FUNCTION PAGE (Page 3)           //
//=========================================//
SPI_W_3BYTE(0x03, 0x00, 0x00);              //** Setting LED driver to shutdown mode
SPI_W_3BYTE(0x03, 0x13, 0xAA);              //** Setting internal channel pulldown/pullup
SPI_W_3BYTE(0x03, 0x14, 0x00);              //** Select scan phase to CB1~CB12
SPI_W_3BYTE(0x03, 0x15, 0x04);              //** Setting PWM Delay Phase enable
SPI_W_3BYTE(0x03, 0x16, 0xC0);              //** Setting CA/CB Channel Slew Rate enable
SPI_W_3BYTE(0x03, 0x1A, 0x00);              //** Setting Iref mode Disable
//=========================================//
// Clear LED CONTROL PAGE (Page 0)          //
//=========================================//
SPI_W_NBYTE(0x00, 0x00, 0x47, 0x00);        //** Clear LED Control Register 0x00~0x47 data
//=========================================//
// Clear PWM PAGE (Page 1)                  //
//=========================================//
SPI_W_NBYTE(0x01, 0x00, 0xBF, 0x00);        //** Clear PWM Register 0x00~0xBF data
//=========================================//
// Set CURRENT PAGE (Page 4)                //
//=========================================//
SPI_W_NBYTE(0x04, 0x00, 0x0B, 0xCC);        //** Setting CCS Register Addr. 0x00~0x0B = 0xCC
```

➢ Switch SNLED2730 LED Effect Algorithm

```
//=========================================//
// Set LED driver to shutdown mode (Page 3) //
//=========================================//
SPI_W_3BYTE(0x03, 0x00, 0x00);              //** Setting LED driver to shutdown mode
//=========================================//
// Set 192 LEDs Control ON/OFF Register (Page 0) //
//=========================================//
SPI_W_NBYTE(0x00, 0x00, 0x17, 0xFF);        //** Setting 192 LEDs Control Register ON
//=========================================//
// Set CURRENT PAGE (Page 4)                //
```

```
//=========================================//
SPI_W_NBYTE(0x04, 0x00, 0x0B, 0x80);          //** Setting CCS Register Addr. 0x00~0x0B = 20mA
//=========================================//
// Clear PWM PAGE (Page 1)                  //
//=========================================//
SPI_W_NBYTE(0x01, 0x00, 0xBF, 0x00);          //** Clear PWM Register 0x00~0xBF data
//=========================================//
// Setting LED driver to normal mode (Page 3)  //
//=========================================//
SPI_W_3BYTE(0x03, 0x00, 0x01);                //** Setting LED driver to normal mode
```

➢ Set SNLED2730 LED Effect Algorithm

```
//=========================================//
// Set LED PWM Effect Algorithm (Page 1)    //
//=========================================//
SPI_W_NBYTE(0x01, 0x00, 0xBF, 0xFF);          //** Setting 192 LEDs PWM Register data to 0xFF
Setting LED Algorithm…
```

➢ Set SNLED2730 to Software Sleep

```
//=========================================//
// Set Software Sleep (Page 3)              //
//=========================================//
SPI_W_3BYTE(0x03, 0x00, 0x00);                //** Setting LED driver to shutdown mode
SPI_W_3BYTE(0x03, 0x1A, 0x02);                //** Setting Software sleep
__Delay(1ms);
```

9 ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATING

Supply voltage (Vdd)..... - 0.3V ~ 5.5V
Input in voltage (Vin)..... Vss – 0.2V ~ Vdd + 0.2V
Operating ambient temperature (Topr)..... -40°C ~ + 85°C
Storage ambient temperature (Tstor) ..... –40°C ~ + 125°C

9.2 ELECTRICAL CHARACTERISTIC

(All of voltages refer to Vss, Vdd = 5.0V, ambient temperature is 25℃ unless otherwise note.)

PARAMETER	SYM.	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	Vdd		2.7*	-	5.5	V
Vdd rise rate	Vpor	Vdd rise rate to ensure internal power-on reset	0.05	-	-	V/ms
Input Low Voltage	ViL	SDB, MISO, ADDR/CS, SCK/SCL, SDA/MOSI, SYSRST pins	Vss	-	0.3*VDD IO	V
Input High Voltage	ViH		0.7*VDD IO	-	VDDIO	V
Input Low Voltage	ViL	MSEL pin.	Vss	-	0.1*VDD	V
Input High Voltage	ViH		0.9*VDD	-	Vdd	V
I/O port input leakage current	Ilekg	Vin = Vdd	-	-	2	uA
Default output current	Iout	Output current of CA1~CA16, Vds=0.5V. (The Constant Current Step setting is 0xCC)	-	32	-	mA
Current sink headroom voltage	V_{HR1}	Isink = 640mA	-	400	-	mV
Current source headroom voltage	V_{HR1}	Isource = 32mA	-	400	-	mV
Supply Current	Idd1	Normal Mode (The Constant Current Step setting is 0xCC)	-	6.1	-	mA
	Idd2	Software Shutdown Mode (The Constant Current Step setting is 0x00)	-	2.1	-	mA
	Idd3	Hardware Sleep Mode (V_{SDB}=0V)	-	1.5	5	uA
	Idd4	Software Sleep Mode (V_{SDB}=VDDIO)	-	1.5	5	uA
LVD Voltage	V_{LVD}	Low voltage reset/indicator level	-	2.55	-	V

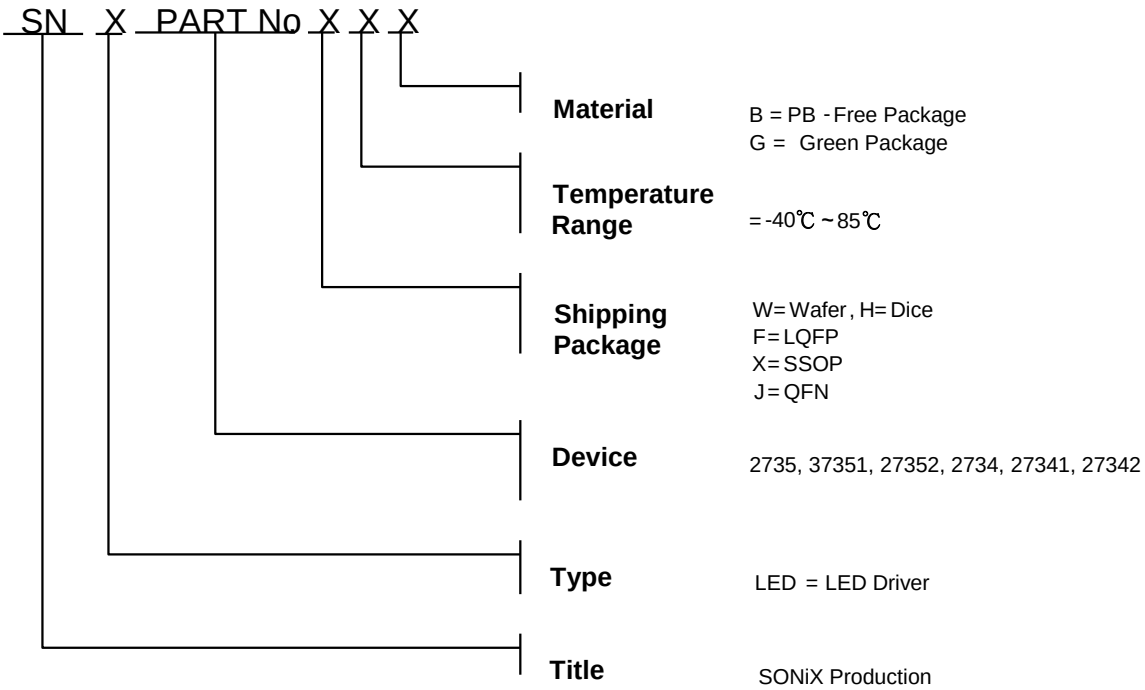
Note 1: Blue LED and Green LED has higher forward voltage. Suggest operating voltage is above 4V.
Note 2: VDDIO ≤ VDD.

10 MARKING DEFINITION

10.1 INTRODUCTION

There are many different types in production line. This note lists the production definition of MCU for order or obtain information.

10.2 MARKING IDENTIFICATION SYSTEM



10.3 MARKING EXAMPLE

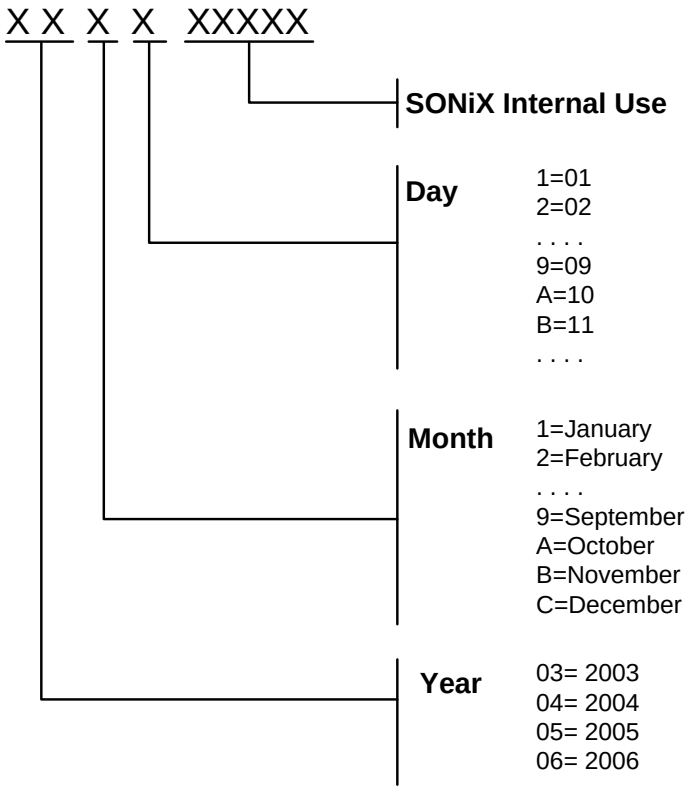
- **Wafer, Dice:**

Name	Type	Device	Package	Temperature	Material
SNLED2735W	ASIC	SNLED2735	Wafer	-40℃~85℃	-
SNLED2735H	ASIC	SNLED2735	Dice	-40℃~85℃	-

- **Green Package:**

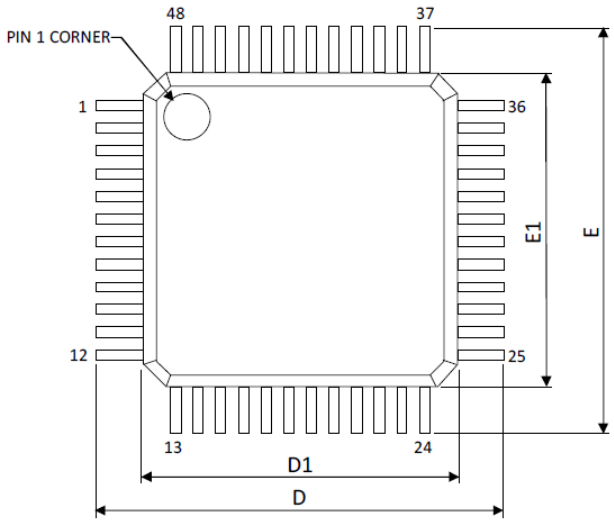
Name	Type	Device	Package	Temperature	Material
SNLED2735F	ASIC	SNLED2735	LQFP	-40℃~85℃	Green Package
SNLED27351J	ASIC	SNLED2735	QFN	-40℃~85℃	Green Package
SNLED27352J	ASIC	SNLED2735	QFN	-40℃~85℃	Green Package
SNLED2734X	ASIC	SNLED2735	SSOP	-40℃~85℃	Green Package
SNLED27341J	ASIC	SNLED2735	QFN	-40℃~85℃	Green Package
SNLED27342J	ASIC	SNLED2735	QFN	-40℃~85℃	Green Package

10.4 DATECODE SYSTEM

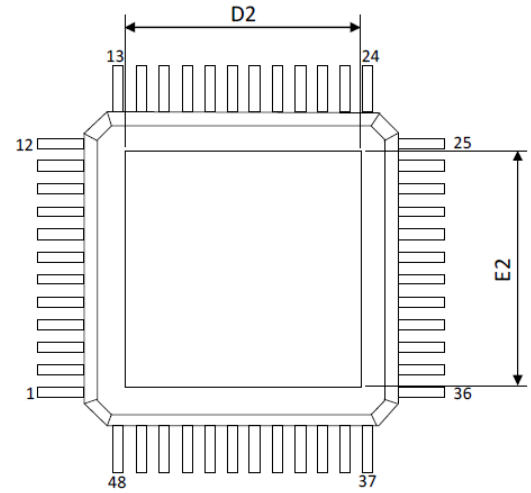


11 PACKAGE INFORMATION

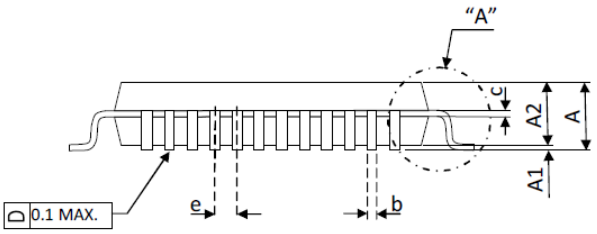
11.1 LQFP 48 PIN (7X7X1.4MM / PITCH：0.5)



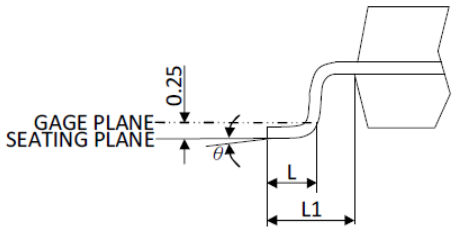
TOP VIEW



BOTTOM VIEW
(THERMALLY ENHANCED VARIATIONS ONLY)



SIDE VIEW



DETAIL "A"

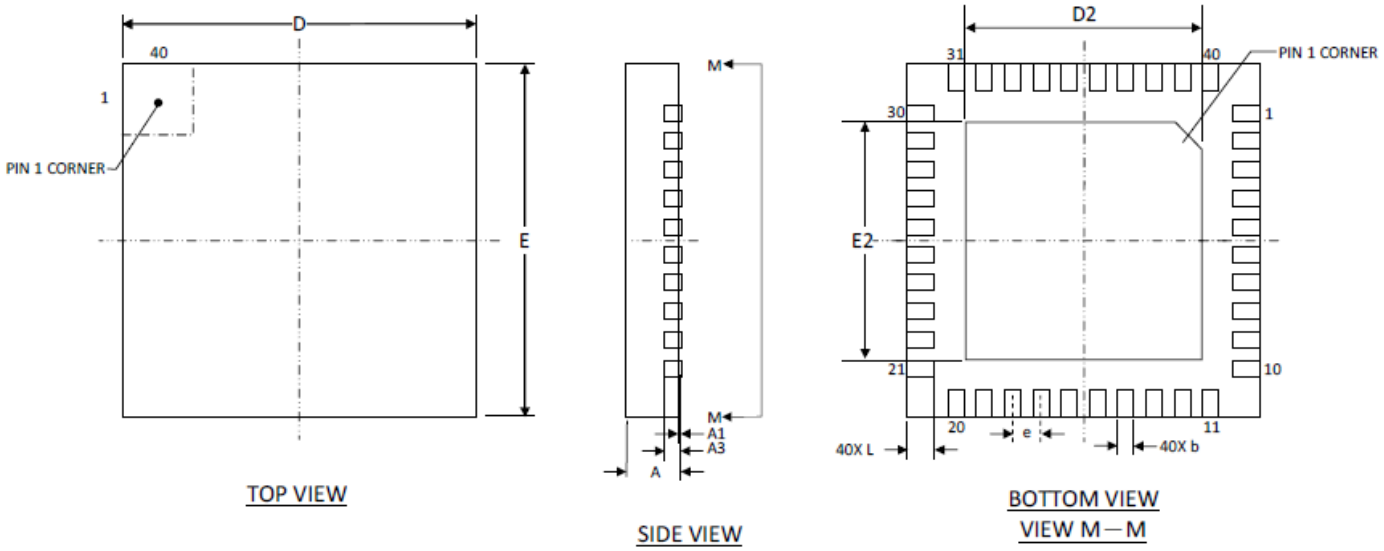
SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	1.60	--	--	0.063
A1	0.05	--	0.15	0.002	--	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	--	0.20	0.004	--	0.008
D	9.00 BSC			0.354		
D1	7.00 BSC			0.276		
E	9.00 BSC			0.354		
E1	7.00 BSC			0.276		
e	0.50 BSC			0.020		
L	0.40	0.60	0.80	0.016	0.024	0.031
L1	1.00 REF			0.039 REF		
θ	0°	3.5°	7°	0°	3.5°	7°

THERMAL ENHANCED DIMENSIONS						
	Dimension in mm			Dimension in inch		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
D2	3.11	4.16	5.21	0.122	0.163	0.205
E2	3.11	4.16	5.21	0.122	0.163	0.205

Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

11.2 QFN 40 PIN (5X5X0.55MM / PITCH：0.4)

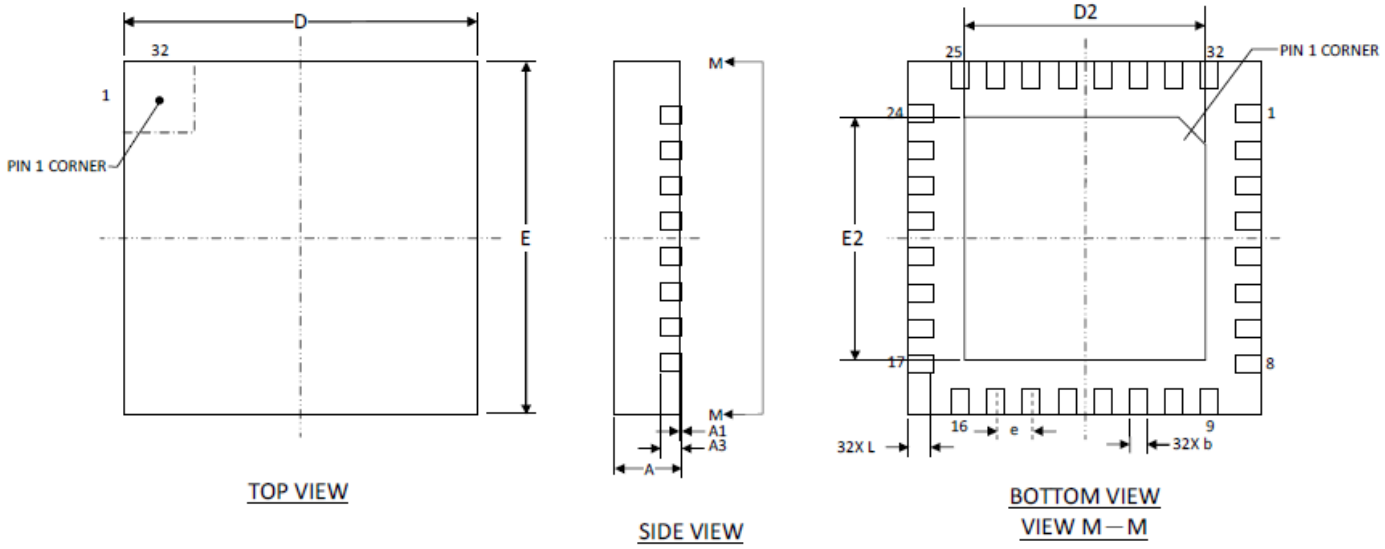


SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.021	0.023
A1	--	0.02	0.05	--	0.001	0.002
A3		0.150 REF			0.006REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		5.00 BSC			0.197 BSC	
E		5.00 BSC			0.197 BSC	
e		0.40 BSC			0.016 BSC	
D2	3.30	3.40	3.50	0.130	0.133	0.137
E2	3.30	3.40	3.50	0.130	0.133	0.137
L	0.25	0.35	0.45	0.010	0.014	0.018

Notes：

1. CONTROLLING DIMENSION：MILLIMETER (mm)

11.3 QFN 32 PIN (4X4X0.55MM / PITCH：0.4)

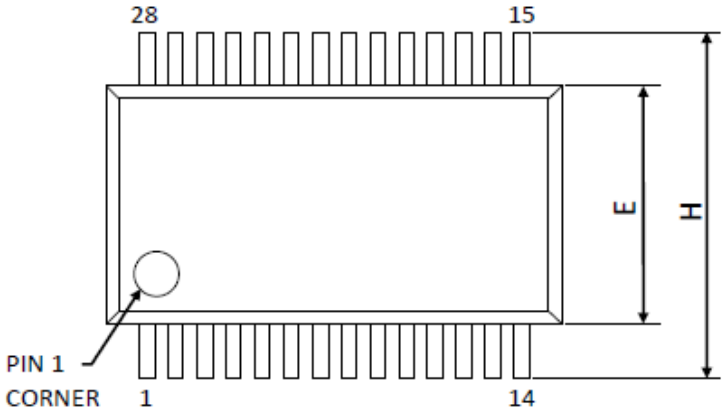


SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0.00	0.02	0.05	0.000	0.000	0.002
A3		0.15 REF			0.006 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		4.00 BSC			0.157 BSC	
E		4.00 BSC			0.157 BSC	
e		0.40 BSC			0.016 BSC	
D2	2.60	2.70	2.80	0.102	0.106	0.110
E2	2.60	2.70	2.80	0.102	0.106	0.110
L	0.25	0.35	0.45	0.010	0.013	0.017

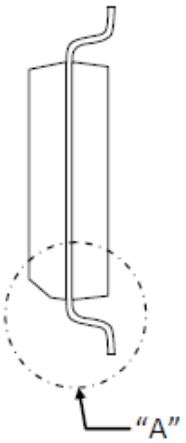
Notes：

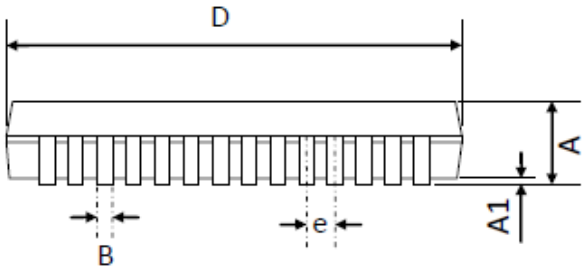
1. CONTROLLING DIMENSION：MILLIMETER (mm)

11.4 SSOP 28 PIN (209MIL)

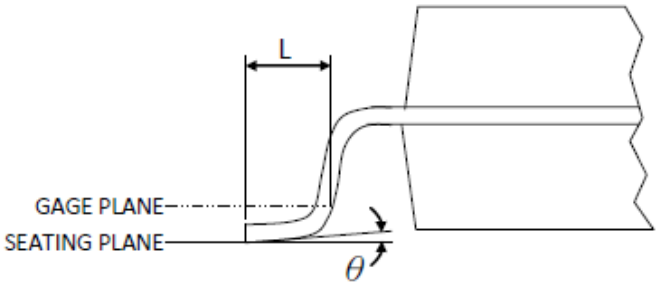


TOP VIEW





SIDE VIEW



DETAIL "A"

SYMBOLS	Dimension in mm			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	--	--	2.0	--	--	0.079
A1	0.05	--	--	0.002	--	--
B	0.22	--	0.38	0.009	--	0.015
D	10.05	10.20	10.50	0.396	0.402	0.413
E	5.00	5.30	5.60	0.197	0.209	0.220
e		0.65 BSC.			0.026 BSC.	
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.55	0.80	1.05	0.022	0.031	0.041
θ	0°	4°	8°	0°	4°	8°

Notes：

1. CONTROLLING DIMENSION：mm
2. JEDEC OUTLINE : MO-105 AH

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